Block diagram of a Schmitt trigger circuit. It is a system with positive feedback in which the output signal fed back into the input causes the amplifier A to switch rapidly from one saturated state to the other when the input crosses a threshold. 

- **A > 1**: amplifier gain
- **B < 1**: feedback transfer function

Comparison of the action of an ordinary comparator and a Schmitt trigger on a noisy analog input signal (U). The output of the comparator is A, and the output of the Schmitt trigger is B. The green dotted lines are the circuit's switching thresholds. The Schmitt trigger tends to remove noise from the input signal.

Use as an oscillator: 

A Schmitt trigger can be used as an oscillator, for instance, by connecting a pair of R and C to the inverting input (pin 2) and the non-inverting input (pin 1) respectively. This configuration can result in an oscillation frequency that is determined by the values of R and C. The oscillation frequency can be calculated using the formula:

\[ f = \frac{1}{2\pi \sqrt{RC}} \]

where \( f \) is the oscillation frequency, \( R \) is the resistance in ohms, and \( C \) is the capacitance in farads.
At \( V_{IN} = V_{IN, L} = 0.18V \)
M5 turns on, M4 still off
\( V_1 = 1.2V \)

At \( V_{IN} = 0.4V \)
Assume M4 on, M5 off, M4 \& M5 in saturation.
Let \( E_{IN} = 0.4V \), then

\[
\frac{k^2_{m} \cdot V_{IN}}{2} \cdot E_{IN} \cdot \left( V_{IN, V_{IN}} \right) \cdot X
\]

\[
= \frac{k^2_{m} \cdot V_{IN}}{2} \cdot E_{IN} \cdot \left( V_{IN} - V_{IN, V_{IN}} \right) \cdot X
\]

\[
= \frac{k^2_{m} \cdot V_{IN}}{2} \cdot \left( V_{IN} - V_{IN, V_{IN}} \right) \cdot E_{IN} \cdot X
\]

It is seen that at this point, M4 is already on. Thus, the previous analysis, which is based on the assumption that M4 is not conducting, can no longer be valid. At this input voltage, node X is being pulled down towards VCC. This can also be seen clearly from the simulation results. We conclude that the upper logic threshold voltage \( V_{THU} \) is approximately equal to 0.62 V.

Next, we consider negative input voltage, i.e., assume that the input voltage is the

\[
\begin{align*}
& \text{Assume from } V_{IN, L} \text{, let } V_{IN, L} = -0.18V. \text{ The pMOS transistors M1 and M2 are off, and M3 is in saturation, thus,} \\
& E_{G1} \left( V_1 \right) - \frac{E_{G1} \left( V_0 \right)}{2} \left( 1 - \left( V_1 - V_{THU} \right) \right) = 0 \\
& V_2 = V_0 = \left[ V_{IN} \cdot \frac{4.46 \cdot 0.972 + V_0 \cdot V_{THU} + V_{THU} \cdot V_0}{1.8} \right] \\
& V_4 = V_3 = \left[ \frac{V_{THU} \cdot 0.972 + V_0 \cdot V_{THU} + V_{THU} \cdot V_0}{1.8} \right] \\
& V_{IN} = \left[ V_{THU} \cdot 0.972 + V_0 \cdot V_{THU} + V_{THU} \cdot V_0 \right] \\
& V_{IN} = V_{THU} = 0.972V \\
& \text{At } V_{IN} = 0.972V, \text{ M1 is at the edge of turning on, M2 is off, and M3 is in saturation.} \\
& \text{The output voltage is still unchanged.} \\
& \text{At } V_{IN} = 1.2V, \text{ M1 is on and in saturation region, M2 is also in saturation, thus,} \\
& E_{G2} \left( V_1 \right) - \frac{E_{G2} \left( V_0 \right)}{2} \left( 1 - \left( V_1 - V_{THU} \right) \right) = 0 \\
& V_2 = V_0 = \left[ V_{IN} \cdot \frac{4.46 \cdot 0.972 + V_0 \cdot V_{THU} + V_{THU} \cdot V_0}{1.8} \right] \\
& V_4 = V_3 = \left[ \frac{V_{THU} \cdot 0.972 + V_0 \cdot V_{THU} + V_{THU} \cdot V_0}{1.8} \right] \\
& V_{IN} = \left[ V_{THU} \cdot 0.972 + V_0 \cdot V_{THU} + V_{THU} \cdot V_0 \right] \\
& \text{The solution of this equation yields} \\
& V_{IN} = 0.972V \\
& \text{Now we determine the gate-to-source voltage of M2 in} \\
& V_{G2} = 0.32 - 0.32 > V_{THU} = -0.46 \\
& \text{which indicates that M2 is still turned off at this point.}
\end{align*}
\]