Adiabatic circuits for low power and PLL(Phase Locked Loop) for high speed communications

2019. 10. 17

Soongsil University
School of Electronic Engineering
Prof. Yong Moon

숭실대학교 Soongsil University

Outline

1. Introduction
2. Low Power Technology
3. Adiabatic Circuits
4. PLL basics
5. Digital Approaches
6. Other Issues

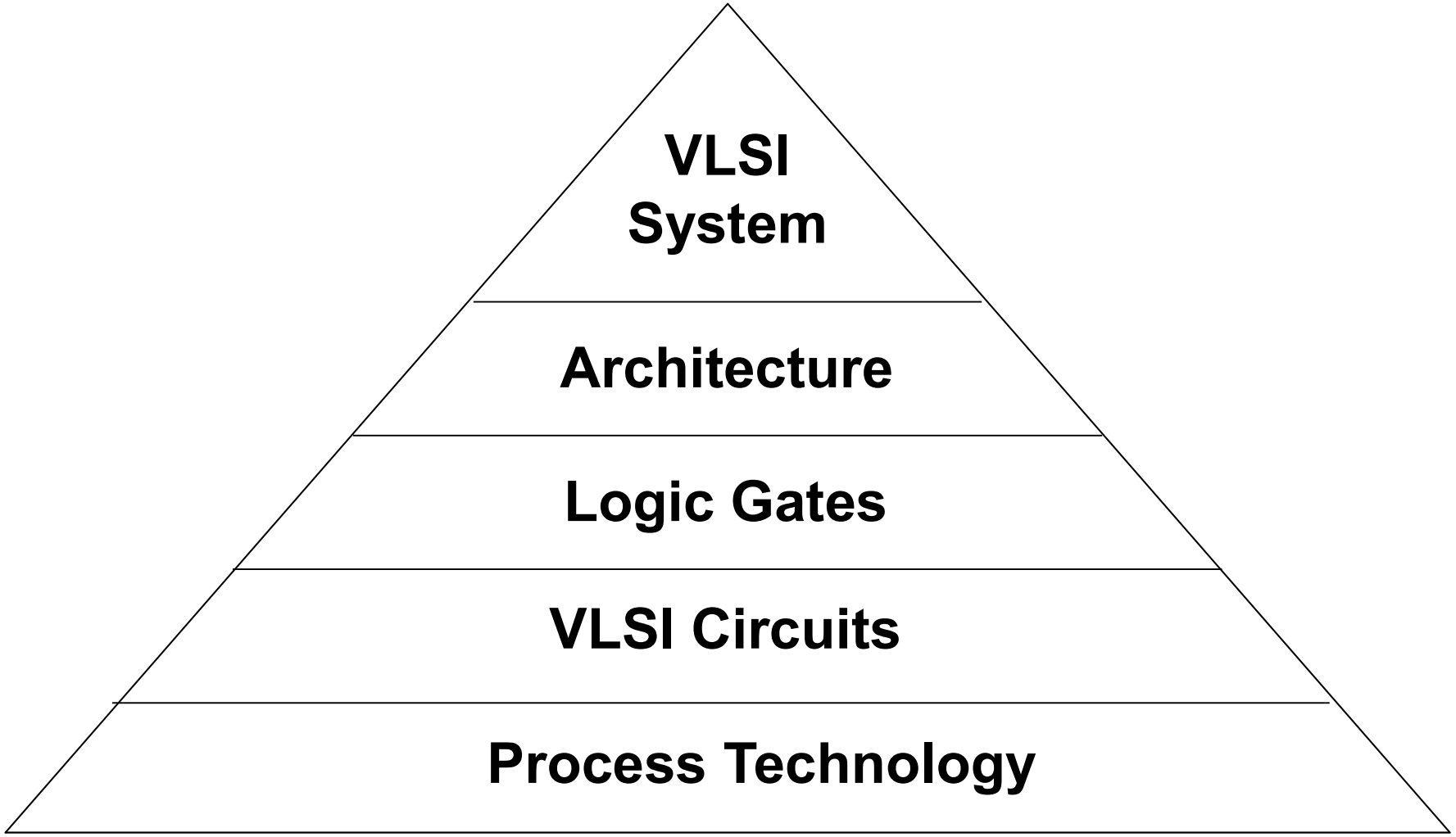
Introduction

- Low power becomes major design goal
  - Battery life for portable system
  - Cooling cost in non-battery powered system
  - Charge loss of conventional static CMOS
  - Leakage power is growing
  - Applications without refueling the energy
- Moore's paper
  - Reliability, cost, complexity, yield
  - And Heat problem → power

Introduction

- Power, Applications and considerations
  - 1-10W: most of applications
    - Cost, performance, package
  - 0.1-1W : mobile, cellular
    - battery, performance, package, cost
  - 10μW-100μW : sensor
    - battery, replacement cost
- Variability problem
  - FFHH vs. TTTH
  - Power : 1.6x
  - Leakage power : 8x

Low Power Technology Hierarchy



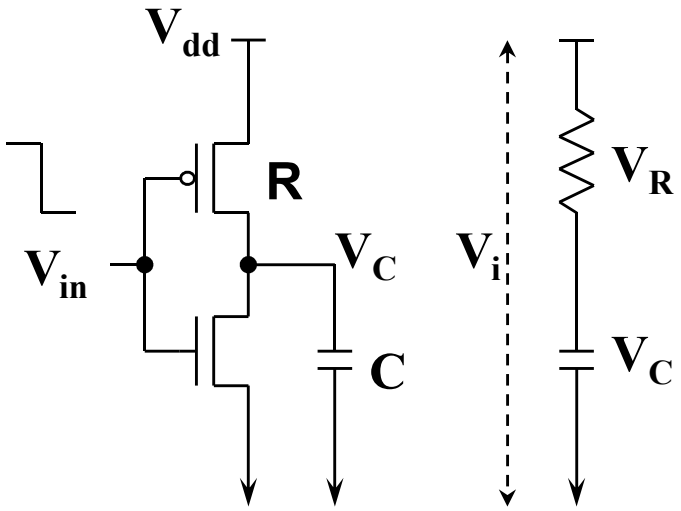
LP System Architecture

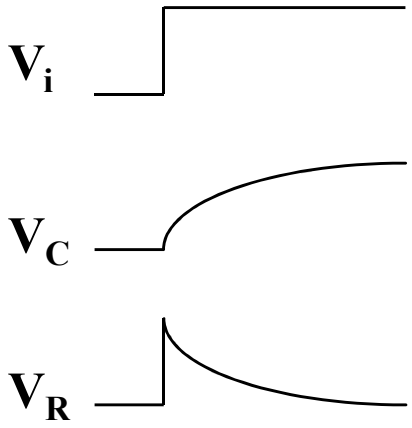
- Low power architecture choices
  - Algorithms
  - Partitioning
    - HW/SW
    - system-level: analog, digital
  - Pipelining
  - Bus, memory
  - DVFS(Dynamic voltage frequency scaling)
  - Multi-VDD design
  - Power gating
  - Clock gating

LP Transistor Level Work

- Leakage reducing techniques
  - Lowering operating voltage
  - Power gating
  - Dual threshold voltage
  - Cell sizing
  - Non-minimum size gate lengths
  - Substrate biasing
  - Stacking transistor
- Reduce gap between automated and custom design

Concept of Adiabatic Circuit

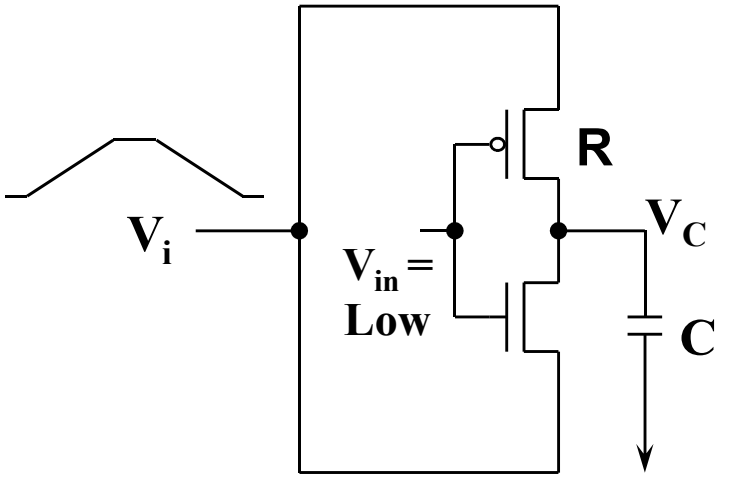


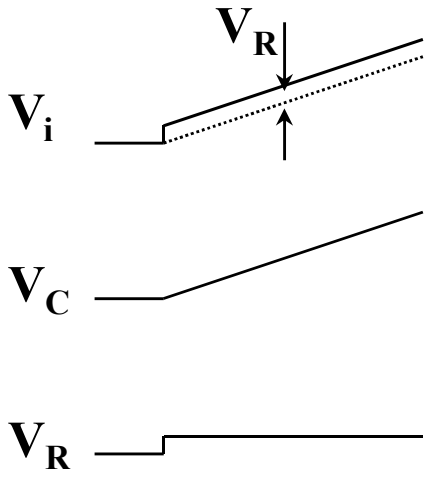


$$E_{Total} = qV_{dd} = CV_{dd}^2$$

$$E_C = CV_{dd}^2/2$$

$$E_R = CV_{dd}^2/2 \quad (heat)$$





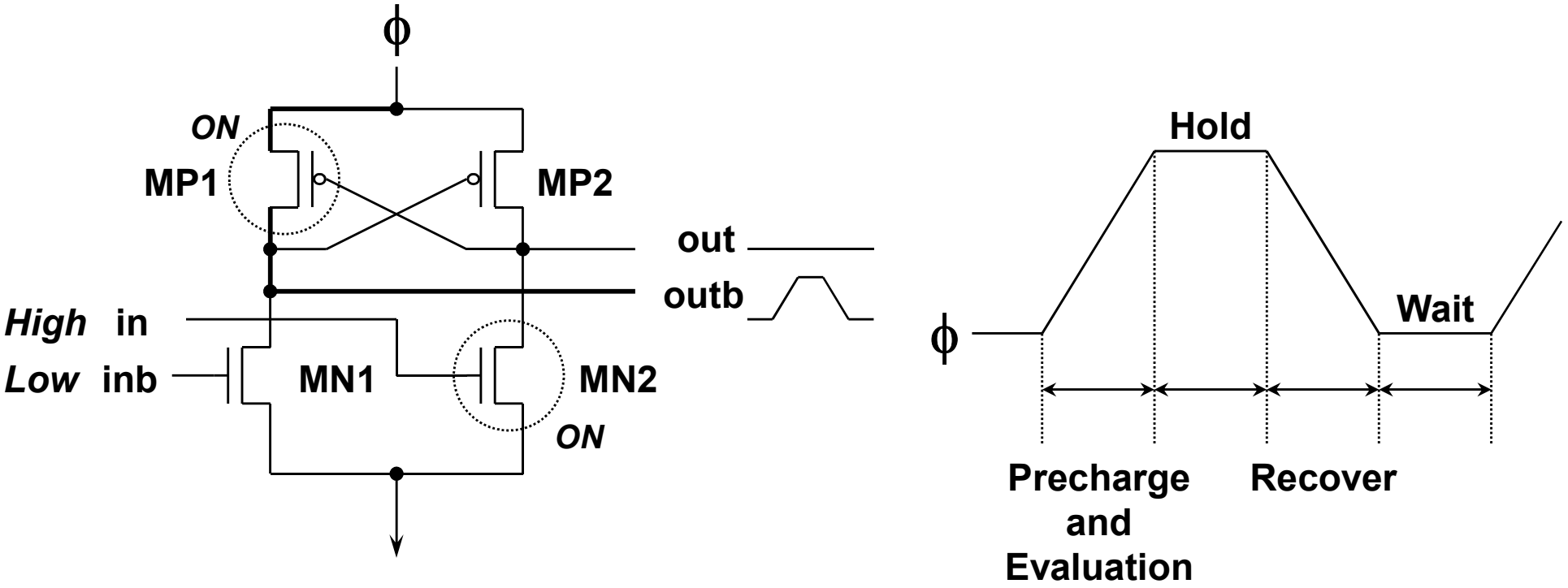
$$E_{diss} = I^2RT = \left(\frac{CV_{dd}}{T}\right)^2 RT = \left(\frac{RC}{T}\right)CV_{dd}^2$$

if $RC \ll T$ *then* $E_{diss} \rightarrow 0$

Returning delivered charge

Using AC supply clock

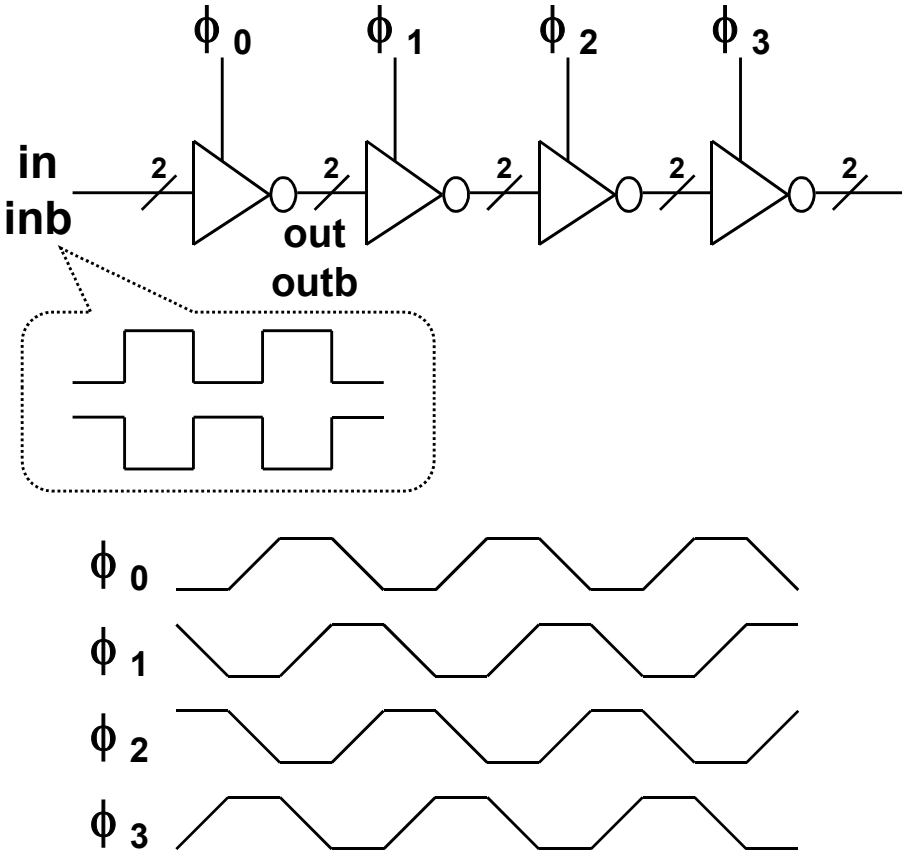
Basic Operation of Adiabatic Circuits

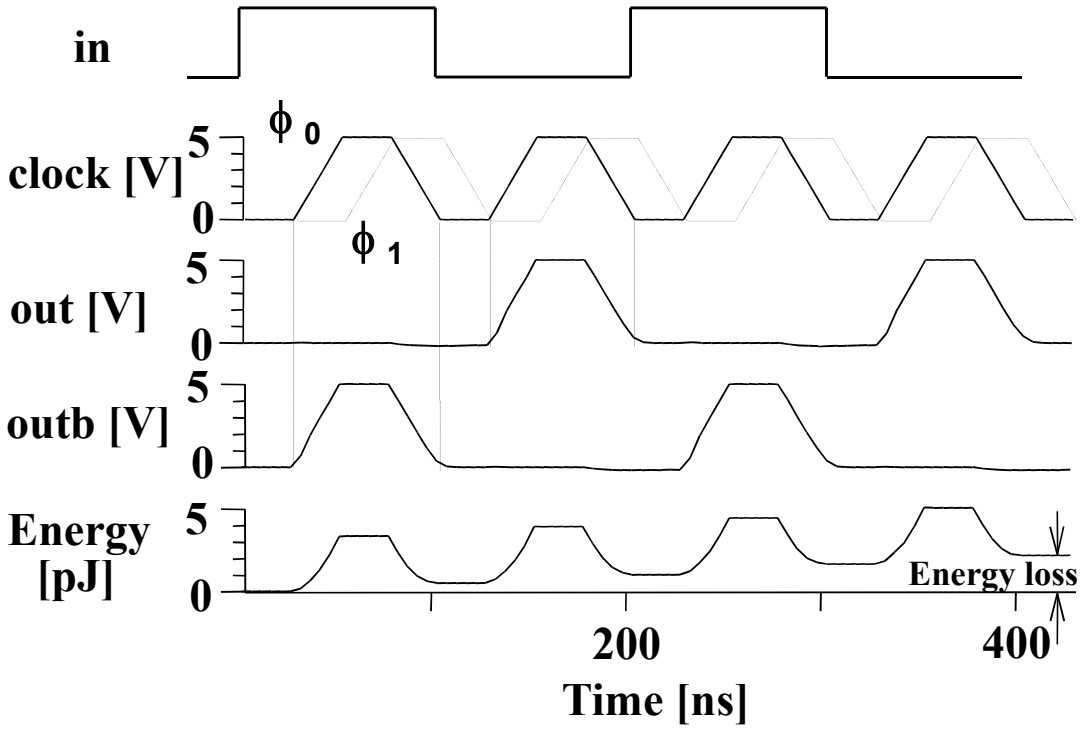


- ECRL(Efficient Charge Recovery Logic)
- Asymptotic energy loss : $E_{ECRL} = C|V_{TP}|^2$

Circuit Construction

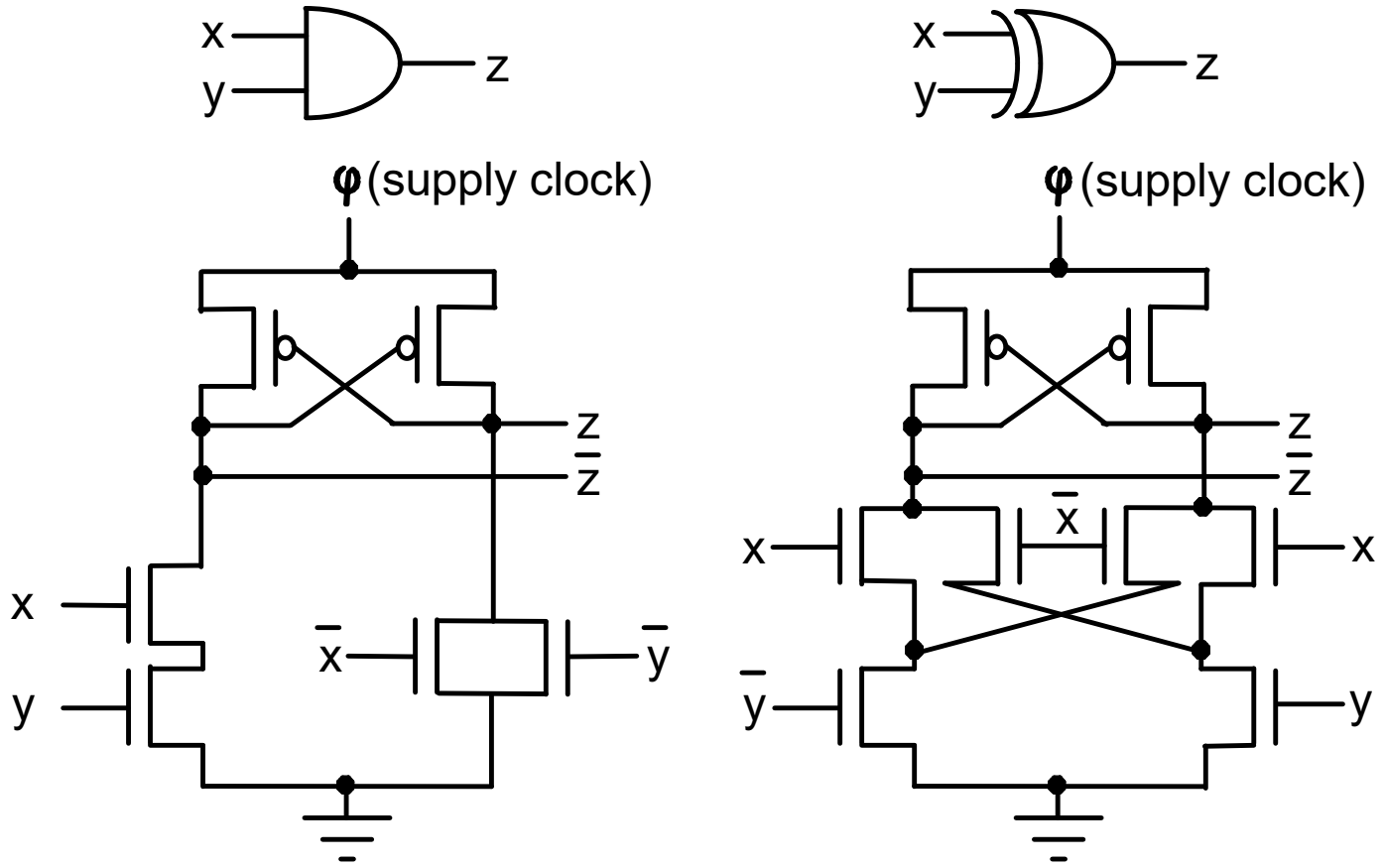
(Inverter Chain)



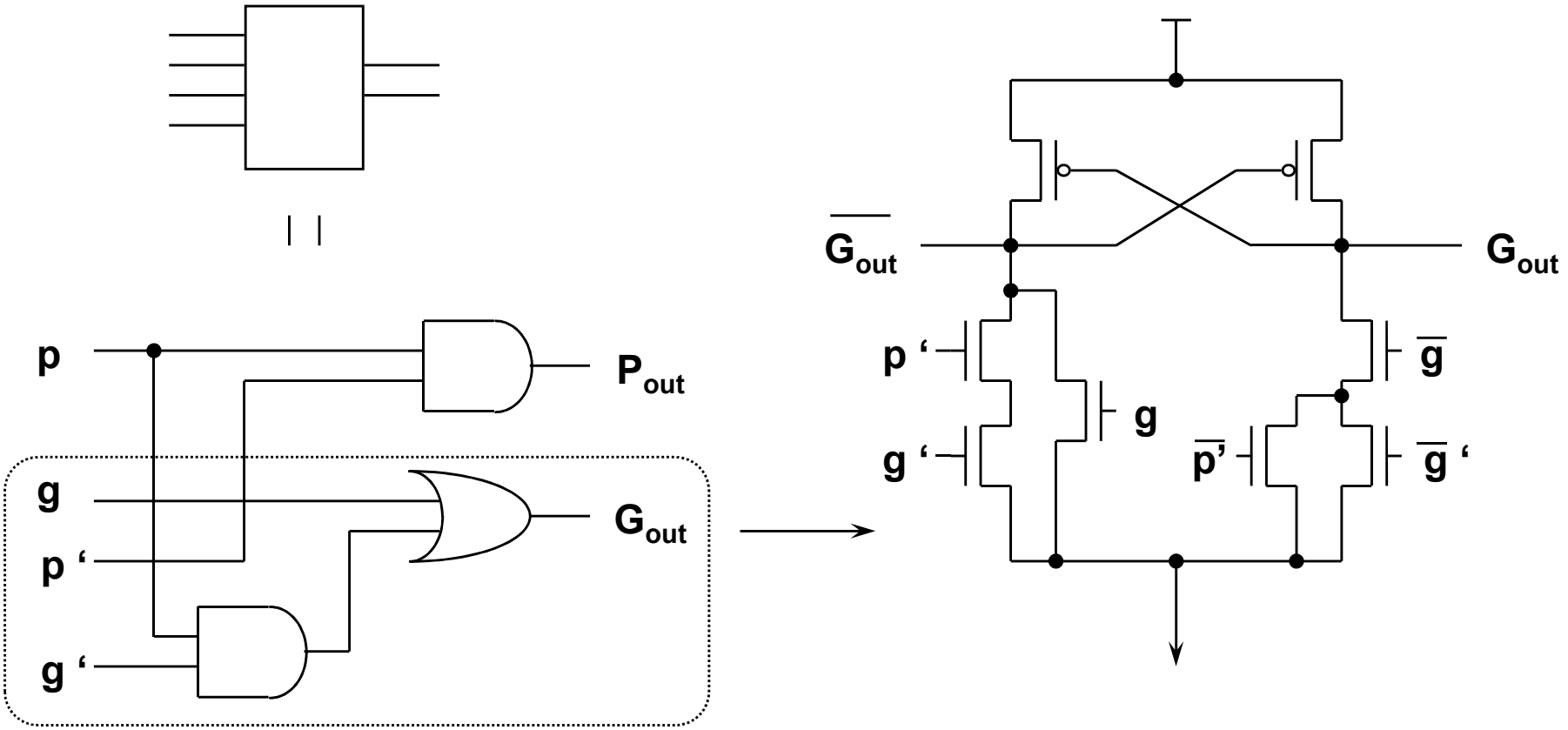


Gate Design

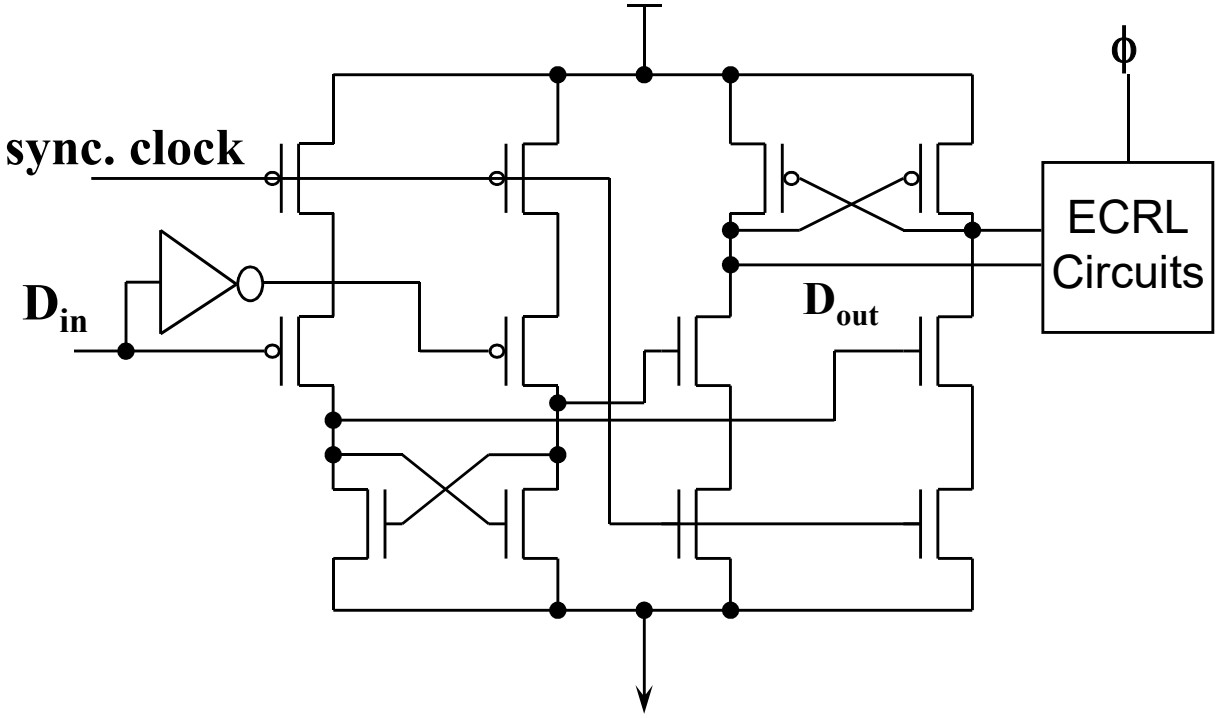
- Same construction as CVSL(Cascode Voltage Switching Logic)



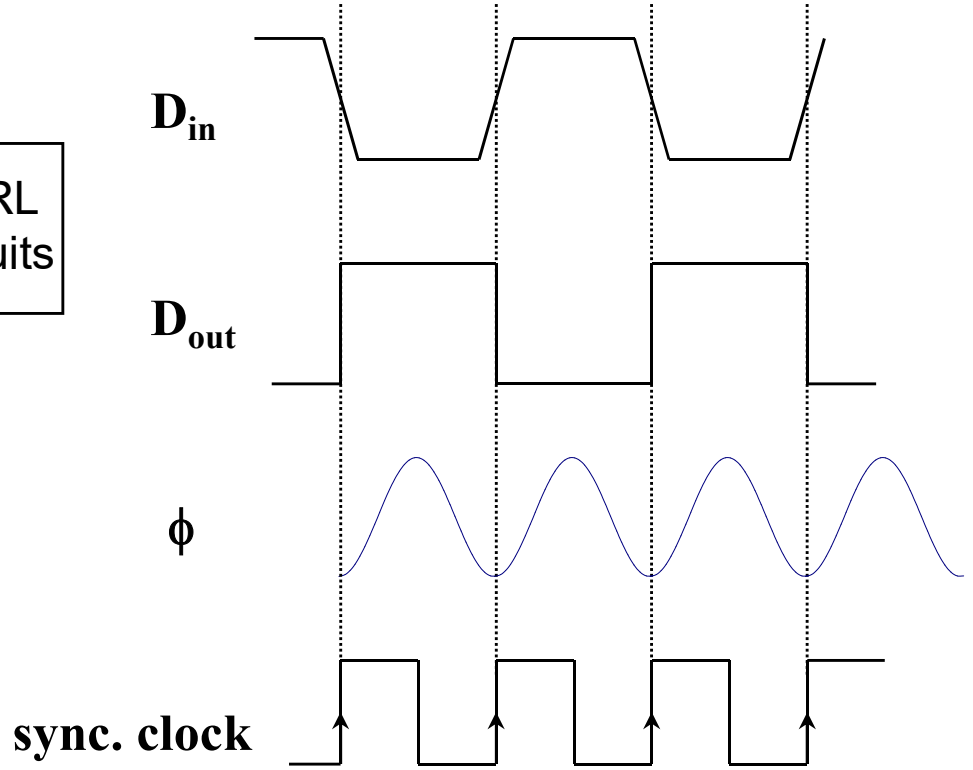
PG Logic for Adder



Interface Circuits

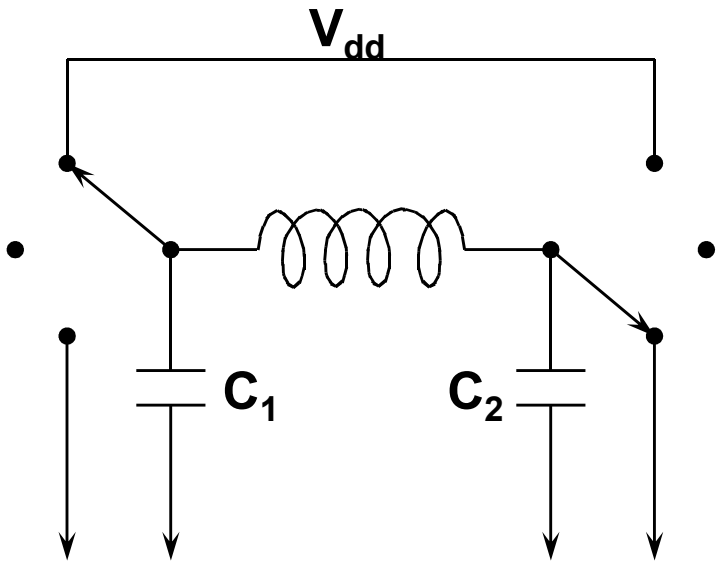


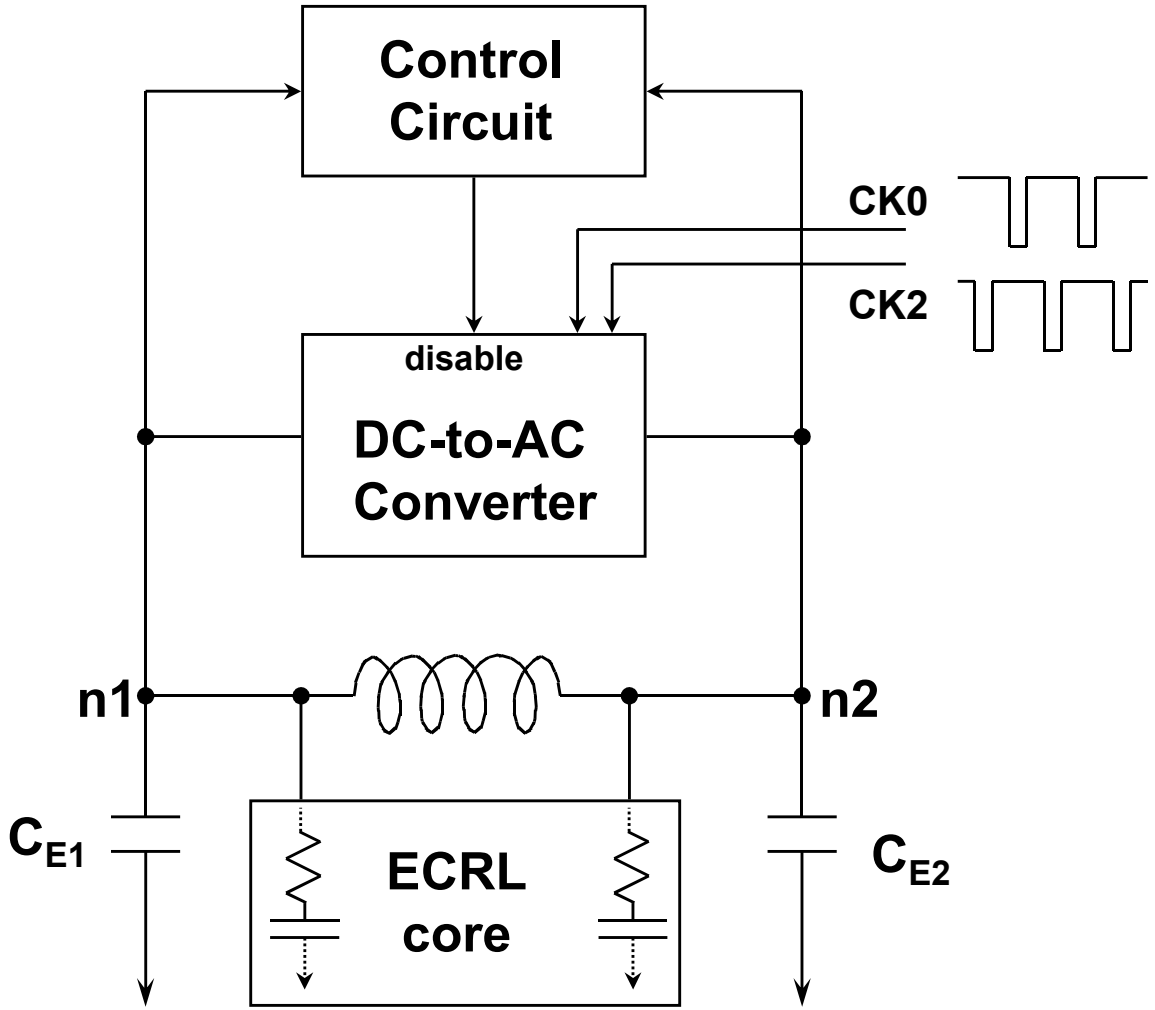
Rising edge-triggered D-type Flip-Flop



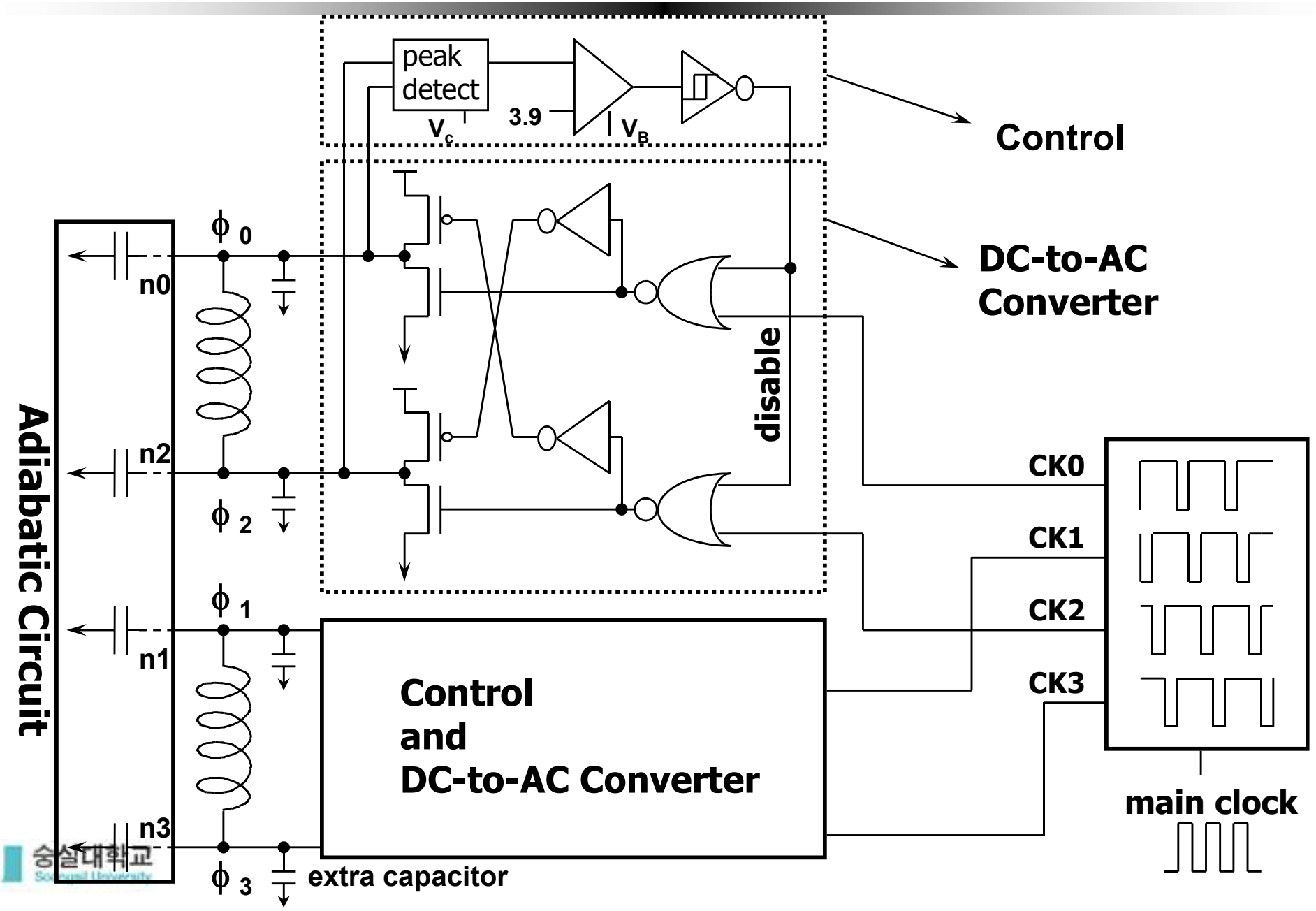
Principles of Clock Circuit

- *LC* resonant circuit





Supply Clock Generator



Energy Efficiency

(16-bit ECRL CLA operating at 10MHz)

Block	Sub-block	Power [uW]		
ECRL core	16-bit adder	258	258	1178
DC-to-AC Converter	NOR gate	27	365	
	Inverter	60		
	MOS switches	278		
Control Circuit	Peak Detector	50	555	
	Comparator	264		
	Schmitt Trigger	241		
Conventional CMOS				1430

Conversion Efficiency = 258/(258+365) = 41%

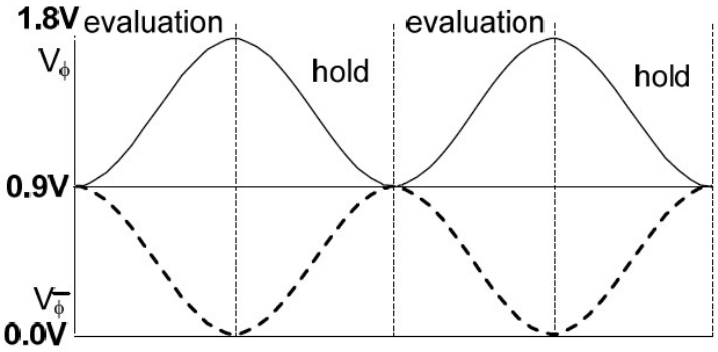
Power Gain over CMOS = 1 - (258+365)/1430 = 56%

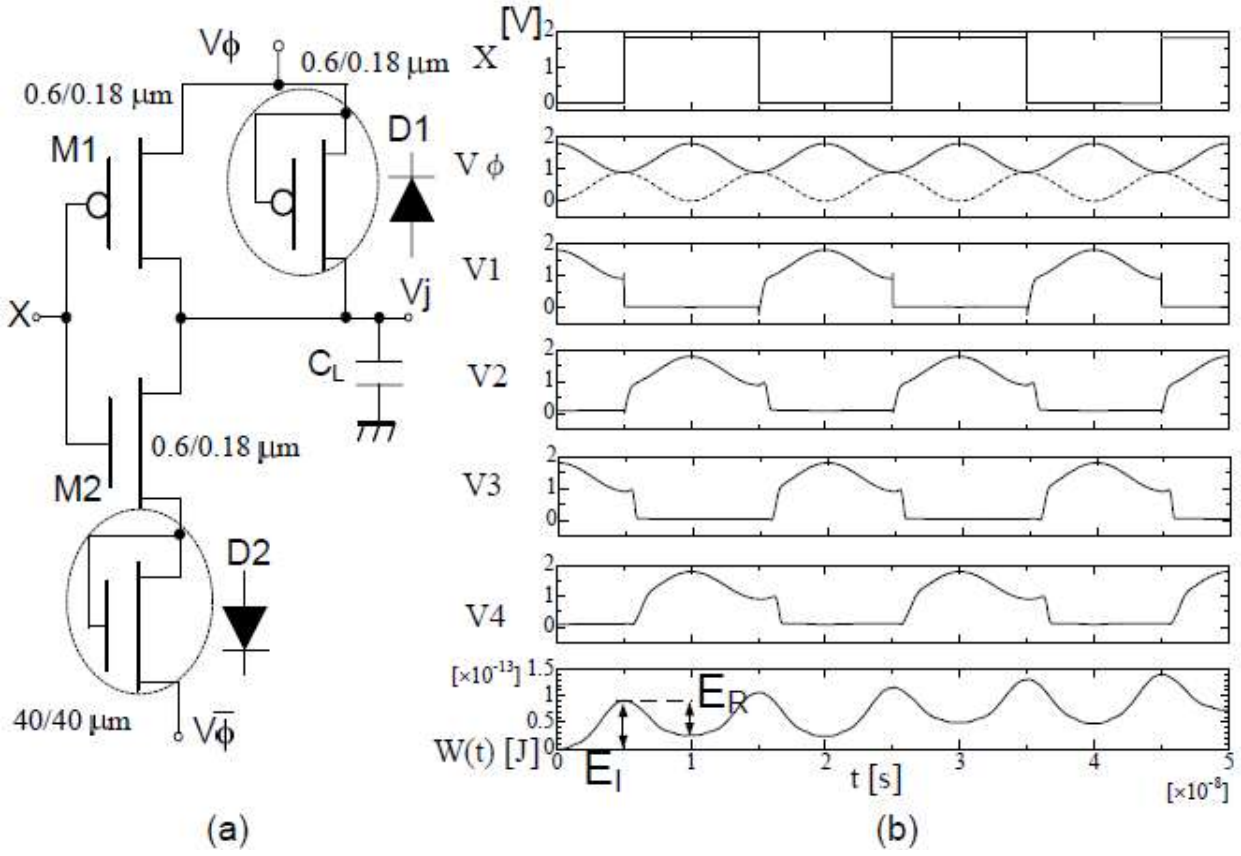
Power Gain over CMOS with Common Block

= 1 - 1178/1430 = 18%

2-Phase Clocked Adiabatic Static CMOS Logic

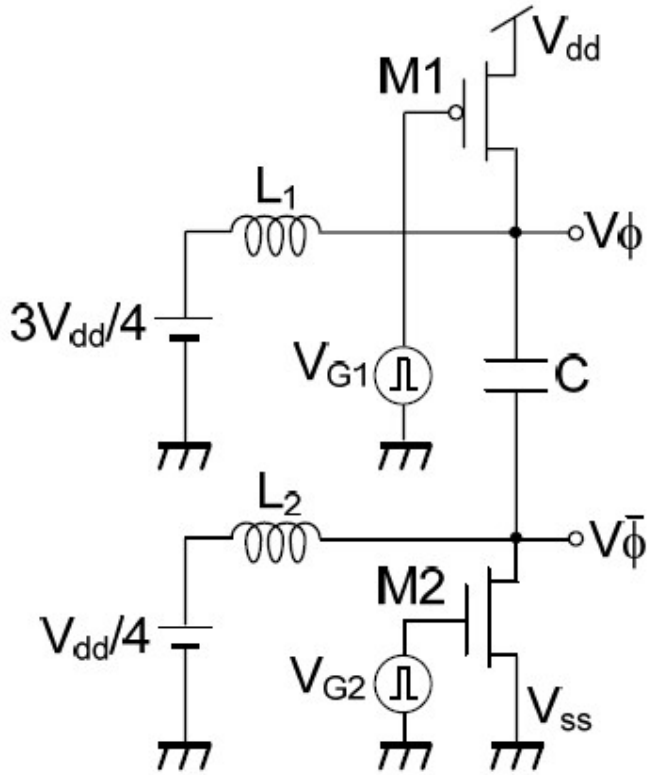
- 2010, Gifu University, Japan
  - 2 complementary split-level sinusoidal power supply clocks (V_{dd})

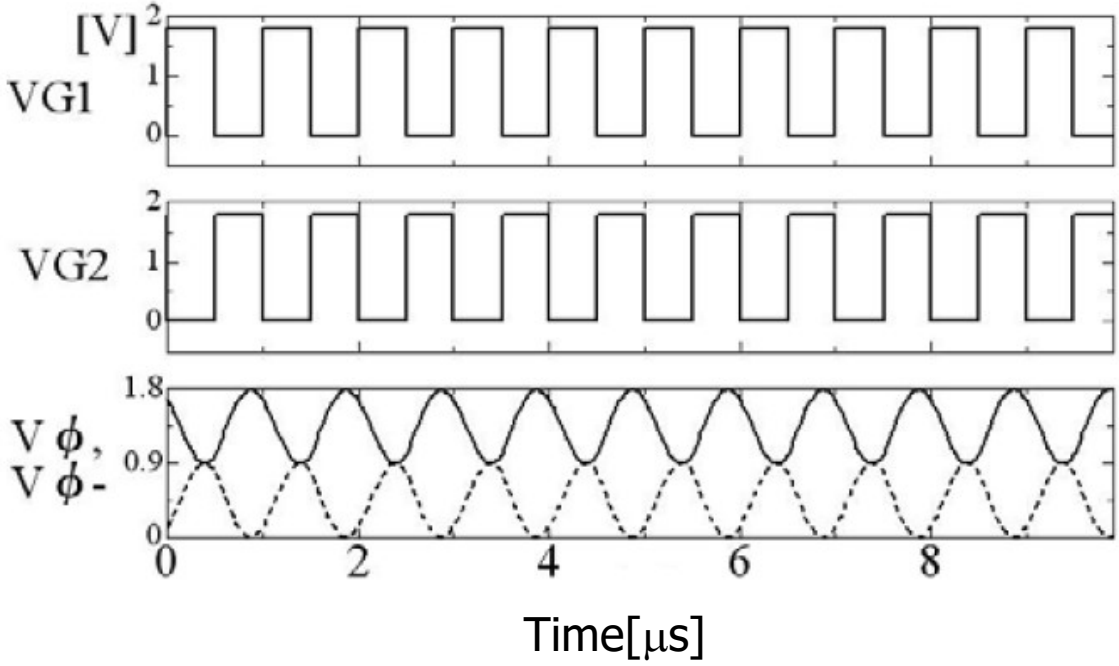




Power Clock Generator

- Simple LC resonant oscillator
- M1, M2 compensate resistive loss
- Voltage regulator with $0.75V_{dd}$ and $0.25V_{dd}$ are used



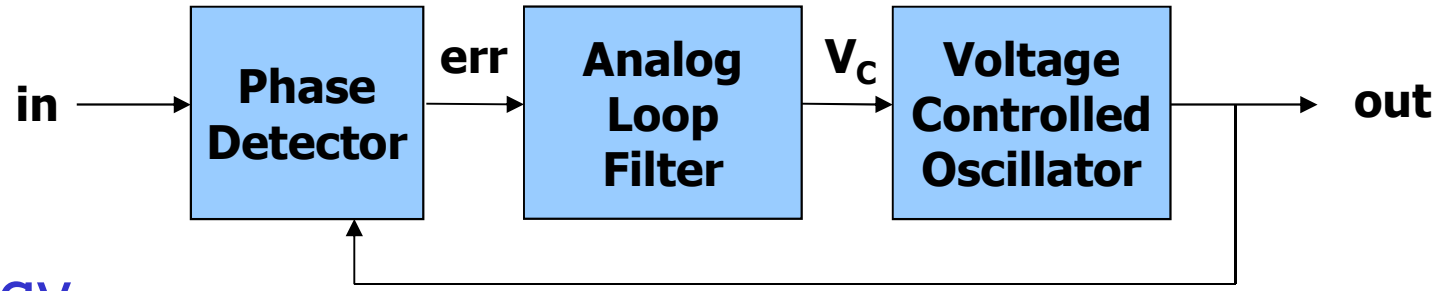


Some Remarks

- Pros
  - Ultra low power dissipation
  - High Fan-out
- Cons
  - Need supply clocks generation
  - C balancing
  - Low operating speed
- Applications
  - RFID, smart cards, sensors
  - Security blocks

PLL(Phase Locked Loop)

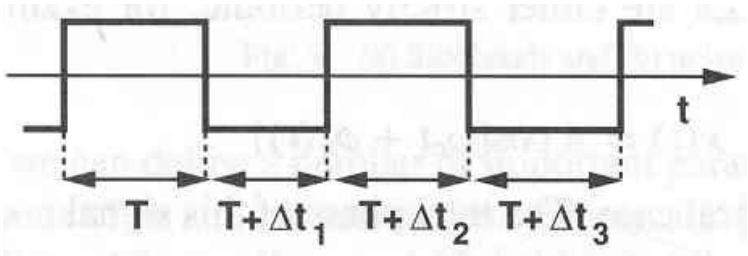
- Definition
  - An oscillator whose phase, and thus frequency is locked to an input signal
- Basic operation
  - The phase detector
    - compares the phases (input signal, internally generated signal)
    - developing a voltage proportional to the phase difference
  - Analog loop filter → smooths PFD signal
  - The voltage is applied to the VCO to reduce the phase difference



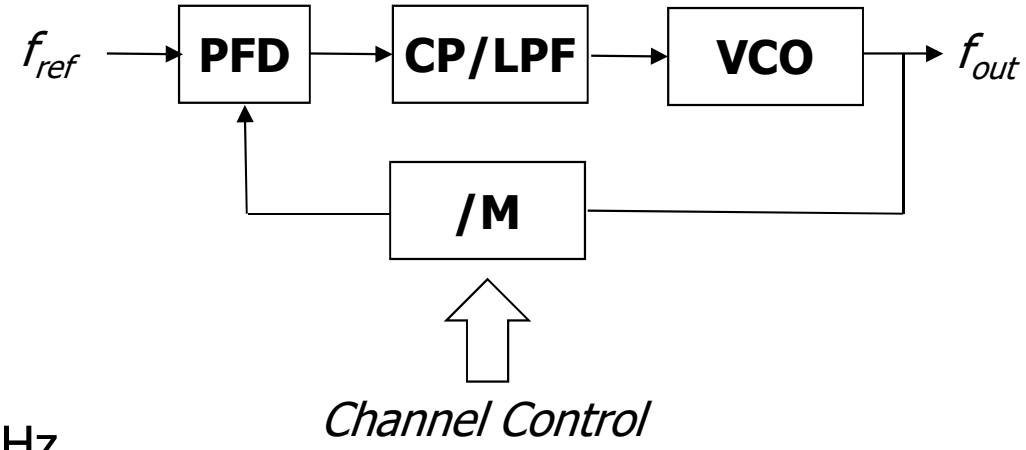
- Analogy
  - Voltage level filtering (low pass filter) vs. Time level filtering

Applications (1)

- Jitter reduction
  - Signals often experience timing jitter as they travel through a communication channel
  - Retrieved from a storage medium

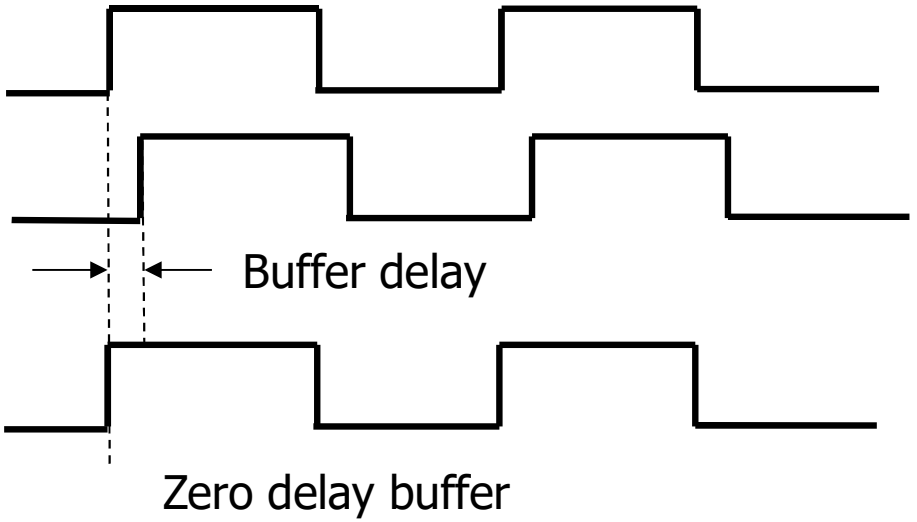


- Frequency multiplication
  - Multiplies input by a factor of M
  - Frequency multiplications at microprocessors
- Frequency Synthesis
  - Accurate periodic waveform
  - Frequency vary in very fine steps
  - Wireless transceivers
    - 900MHz~925MHz in steps of 200KHz

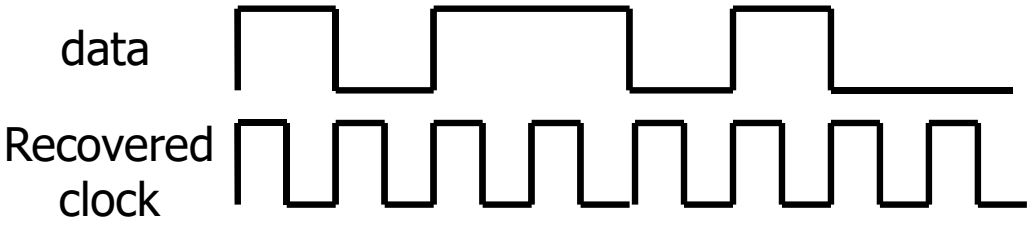


Applications (2)

- Skew suppression
  - Remove the clock buffer delay at digital systems

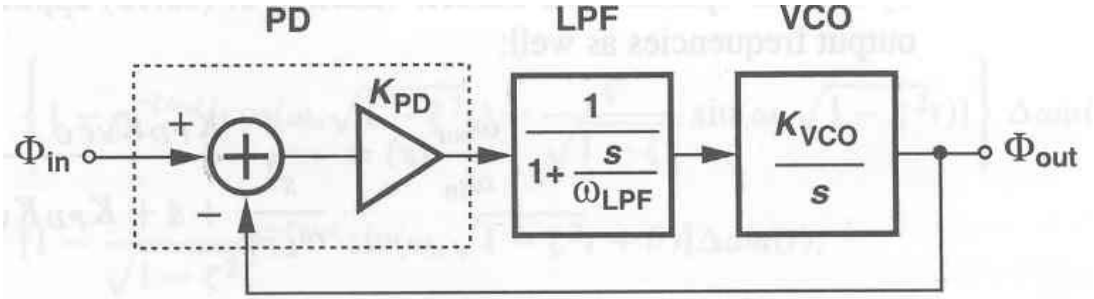


- Clock Recovery
  - Data is transmitted without any additional timing reference
  - The timing information must be recovered from the data at the receive end

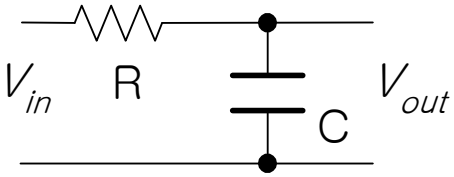


2nd order System

- Linear model of type I PLL



single pole LPF



  - 1st order LPF, PD(subtractor with amplification), …
  - Open-loop transfer function

$$H(s)\Big|_{\text{open}} = \frac{\Phi_{out}}{\Phi_{in}}(s)\Big|_{open} = K_{PD}\frac{1}{1+\frac{s}{\omega_{LPF}}}\frac{K_{VCO}}{s}$$

  - Close-loop transfer function

$$H(s)\Big|_{\text{closed}} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}$$

Loop Dynamics

- 2nd order transfer function and damping factor

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \omega_n = \sqrt{\omega_{LPF} K_{PD} K_{VCO}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD} K_{VCO}}}$$

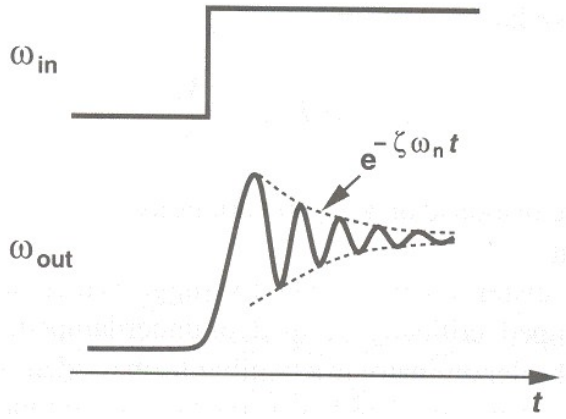
  - Two poles

$$s_{1,2} = -\zeta\omega_n \pm \sqrt{(\zeta^2 - 1)\omega_n^2} = (-\zeta \pm \sqrt{\zeta^2 - 1})\omega_n$$

  - Real pole : overdamped (ζ>1)
  - Complex pole and response to an input frequency step

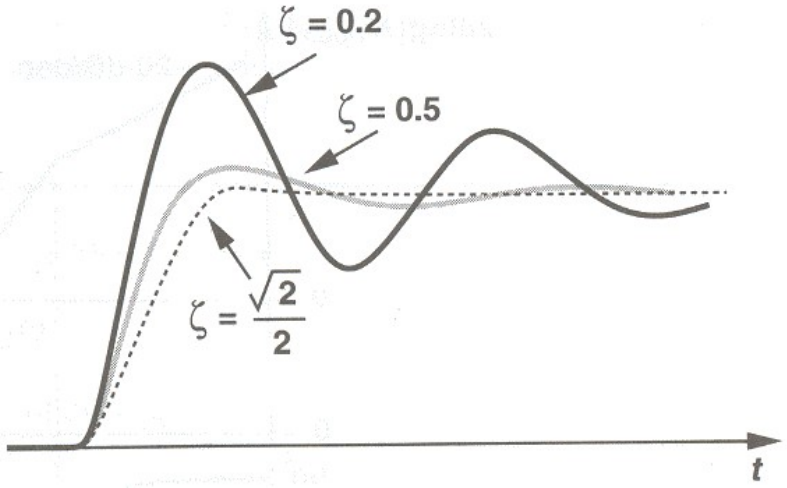
$$\omega_{out}(t) = [1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin(\omega_n\sqrt{1-\zeta^2}t + \theta)]\Delta\omega u(t)$$

$$\theta = \sin^{-1}\sqrt{1-\zeta^2} \qquad \zeta\omega_n = \frac{1}{2}\omega_{LPF} = \frac{1}{\tau_{decay}}$$

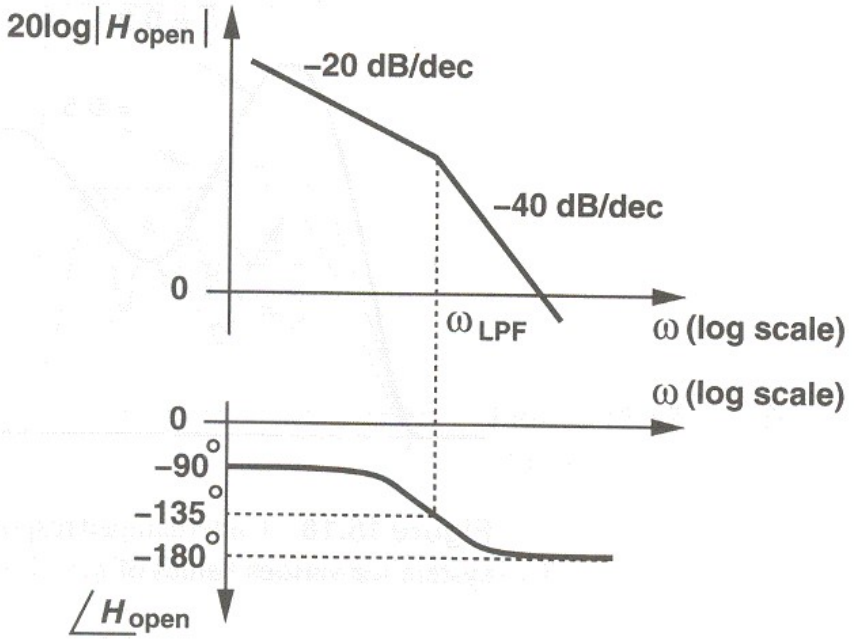


Damping Factor & Stability

- Underdamped response
  - ζ=0.707: maximally flat response
  - ζ=0.707~1 generally used



- Bode plot
  - Mostly unstable
  - Direct relationship among variables
  - Loop gain increase → settling behavior degrades



Voltage Controlled Oscillator

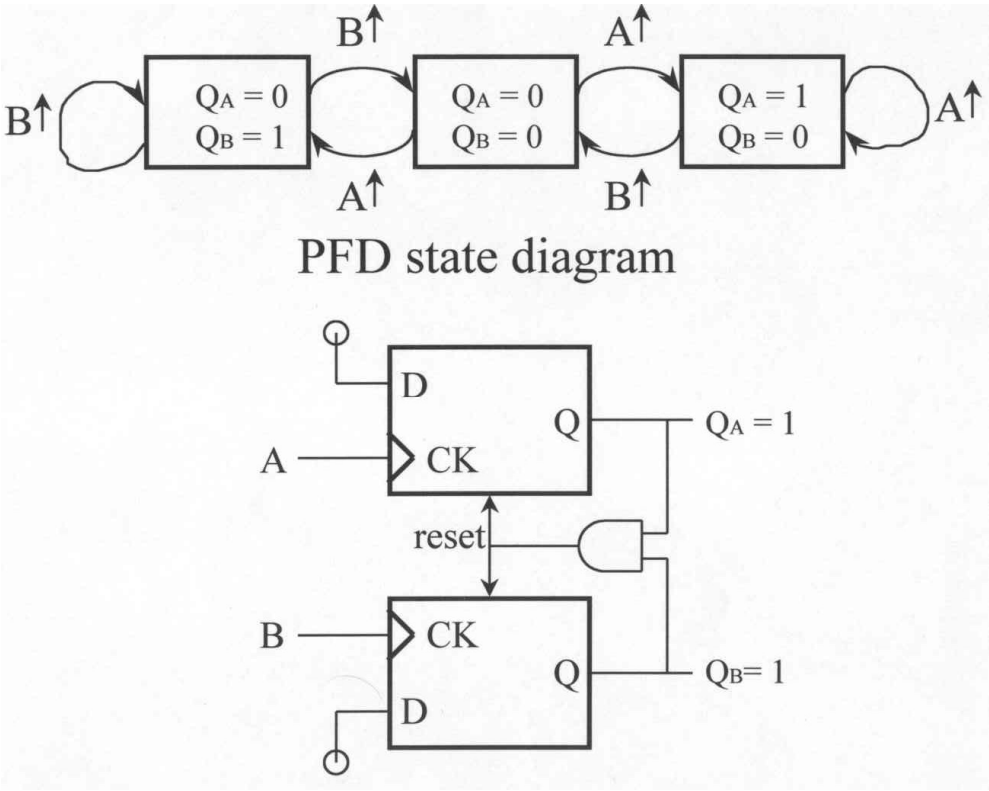
- Parameters to consider
  - Tuning range
    - MIN ~ MAX frequency *vs.* input frequency range
    - Covers the process, temperature and supply variations
  - Jitter
    - Timing accuracy
  - Phase noise
    - Spectral purity
  - Supply and substrate noise rejection
  - Input/output linearity
- Other considerations
  - Single-ended vs. differential
  - Duty cycle

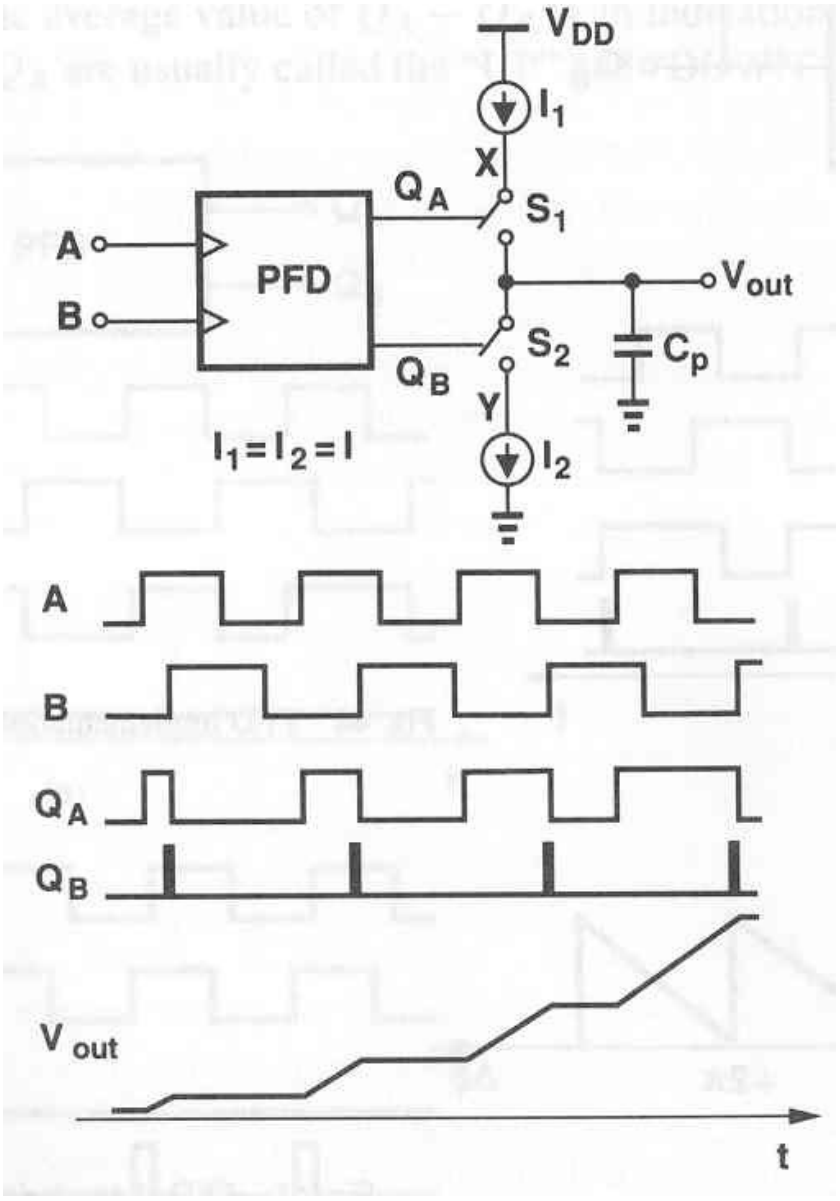
PFD and Charge Pump

- **PFD & Charge Pump**
  - Produce a signal current proportional to the difference in phase or frequency between two input signals
  - Design Issues
    - Gain & Linearity
    - Dead zone
    - Mismatch between sourcing and sinking current
    - Mismatch between UP and DOWN switching time
    - UP/DOWN current programmable
    - Leakage current
    - Maximize voltage compliance

Common Circuits

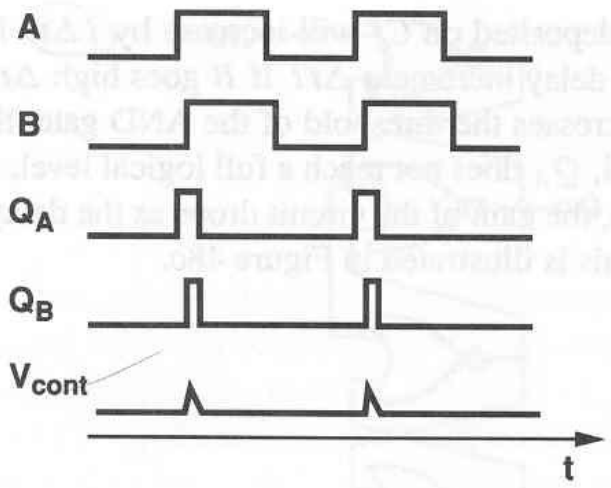
- PFD output
  - Difference amplification → LPF
  - Drive 3-state "charge pump"



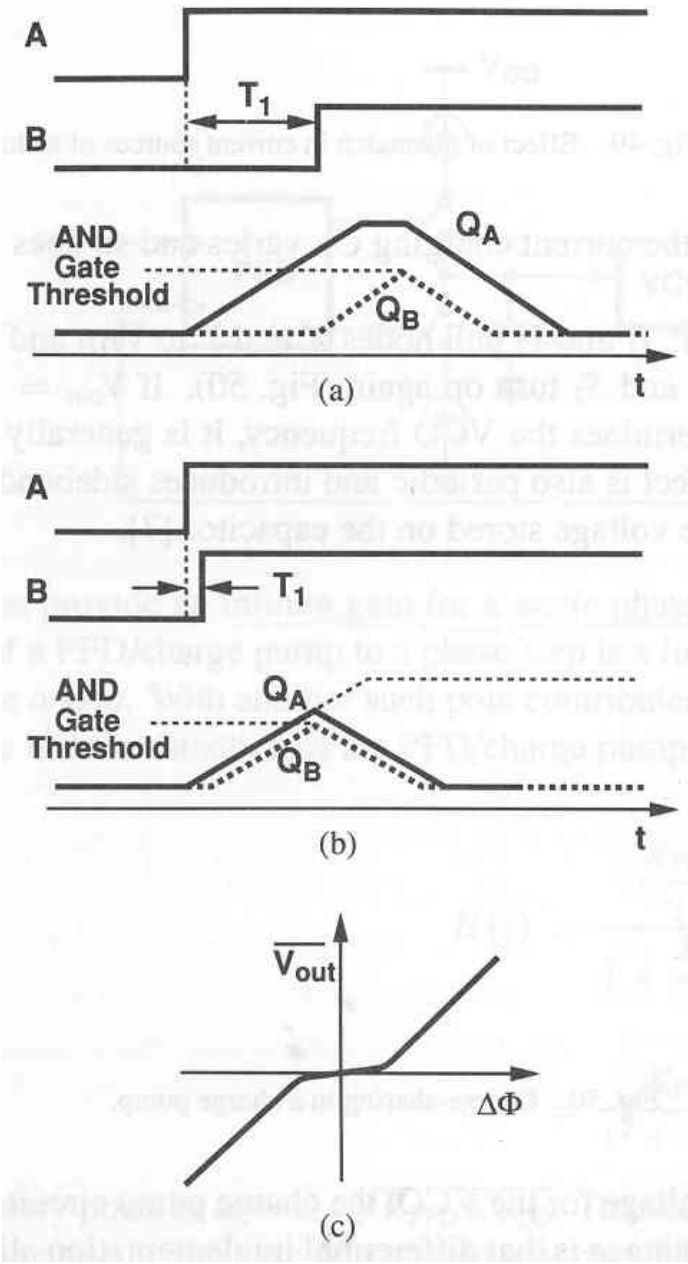


CP & Dead Zone

- Charge pump
  - Infinite DC gain
  - Offset, mismatch
  - Time difference → 0 : gain reduced
  - Input/output difference < dead zone
    - Error occurs
  - Sideband of VCO

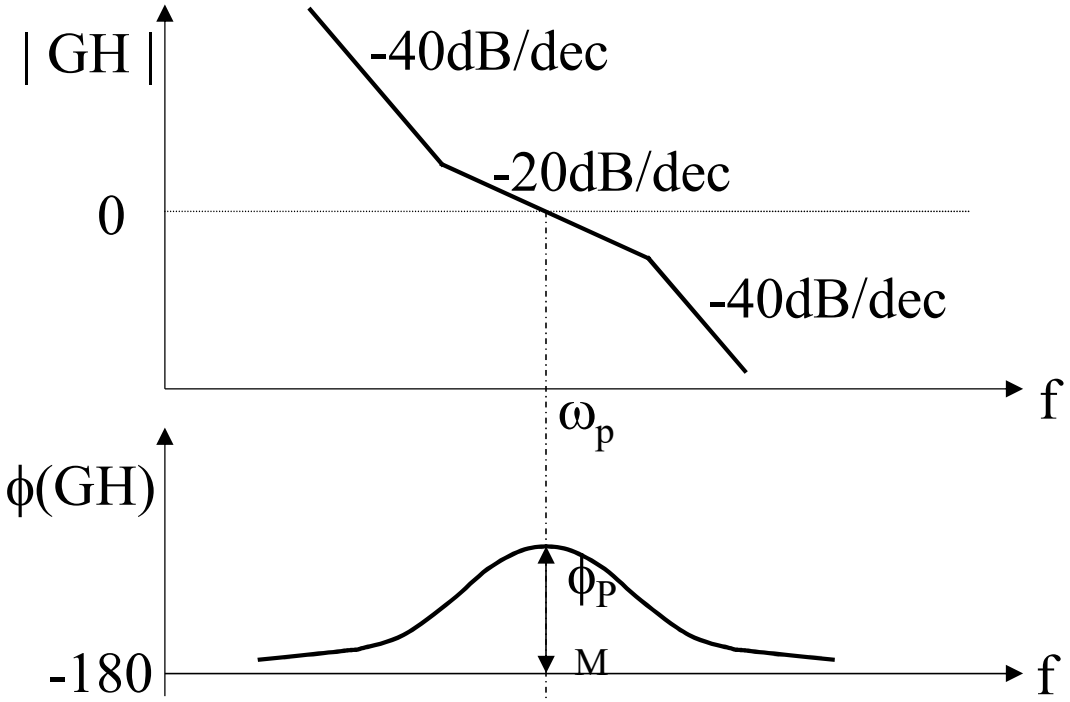


Mismatch in current



Loop Filter & Loop Bandwidth

- Loop Filter
  - Design Tradeoffs
    - The narrower the loop BW
      → the lower reference spurs, but the longer the lock time
    - The wider the loop BW → the phase noise of VCO is limited
- Loop Bandwidth and phase margin



- Loop BW $< \frac{F_{PFD}}{10}$
- Phase Margin $> 50^{o}$

$$for\ \phi_{PM} = 60^{\circ}$$

$$R_2 = \frac{N\omega_p}{K_{pd}K_{VCO}},\ C_2 = \frac{4}{R_2\omega_p}$$

$$C_1 = \frac{1}{4R_2\omega_p}$$

$$\rightarrow\ \omega_p \approx \frac{K_{pd}K_{VCO}}{N}\frac{R_2C_2}{C_1 + C_2}$$

Noise in PLLs

- Jitters
  - Period experiences small changes, Deviating from their ideal points
  - slow jitter and fast jitter
- All the loop components may contribute output phase noise, θ_o.
  - The noise in θ_o should be suppressed.
- Two important cases
  - Input signal contains noise: Bandwidth should be low
  - VCO introduces noise : dominant, Bandwidth should be large

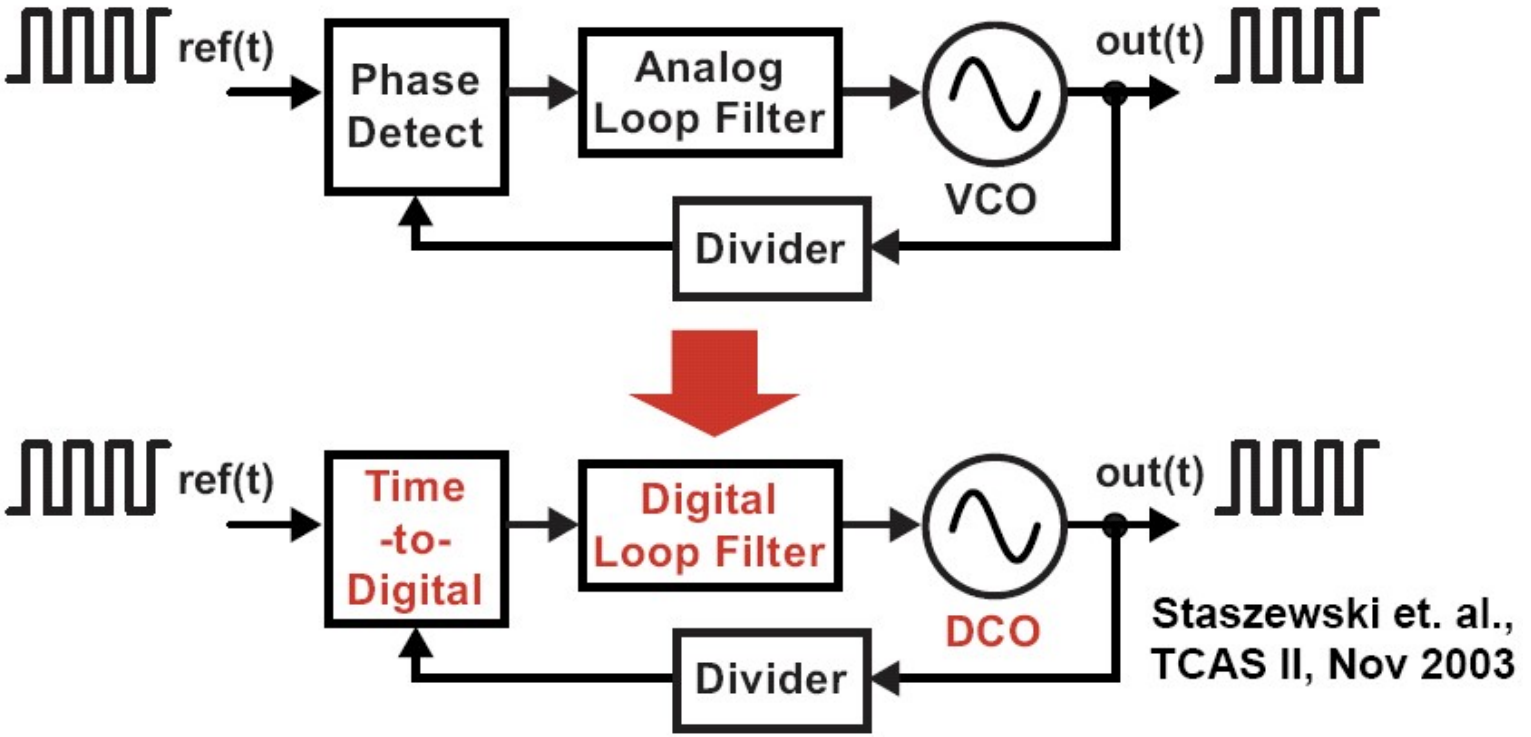
$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{\frac{I_P}{2\pi C}(RCs+1)Kvco}{s^2 + \frac{I_P}{2\pi}KvcoRs + \frac{I_P}{2\pi C}Kvco} = H(s) \qquad \frac{\theta_o(s)}{\theta_{VCO}(s)} = \frac{s^2}{s^2 + \frac{I_P}{2\pi}KvcoRs + \frac{I_P}{2\pi C}Kvco} = H(s)$$

- Increasing the bandwidth of the PLL can lower the contribution of the VCO phase noise

All-Digital PLL

- Demand for digitization of PLL
  - Integrated on IC as a key circuit
  - Elimination of externally attached components
  - No need for adjustment
- Advantages
  - Testability, Programmability, Stability
  - Portability over different processes
  - Reduce the system turn around time
  - Fast lock time
- Disadvantages
  - Need high frequency clock source, low jitter performance
  - Lower frequency range : ADC, counter, …

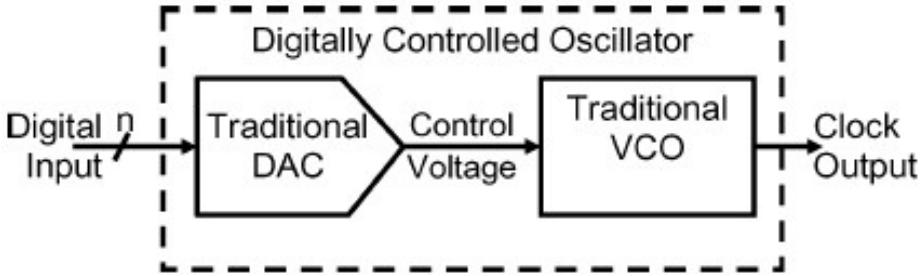
Analog PLL vs. Digital PLL

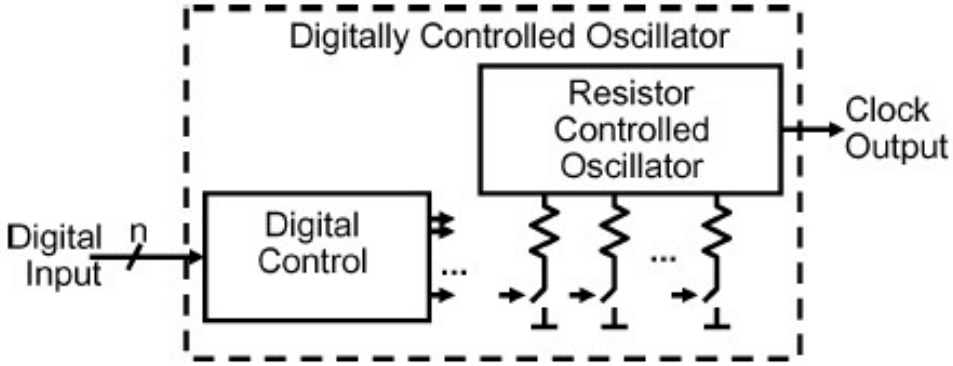


- Digital loop filter
  - Compact area, Leakage insensitive
- Challenges
  - DCO: Digitally Controlled Oscillator
  - TDC: Time-to-Digital Converter

DCO(Digitally-Controlled Oscillator)

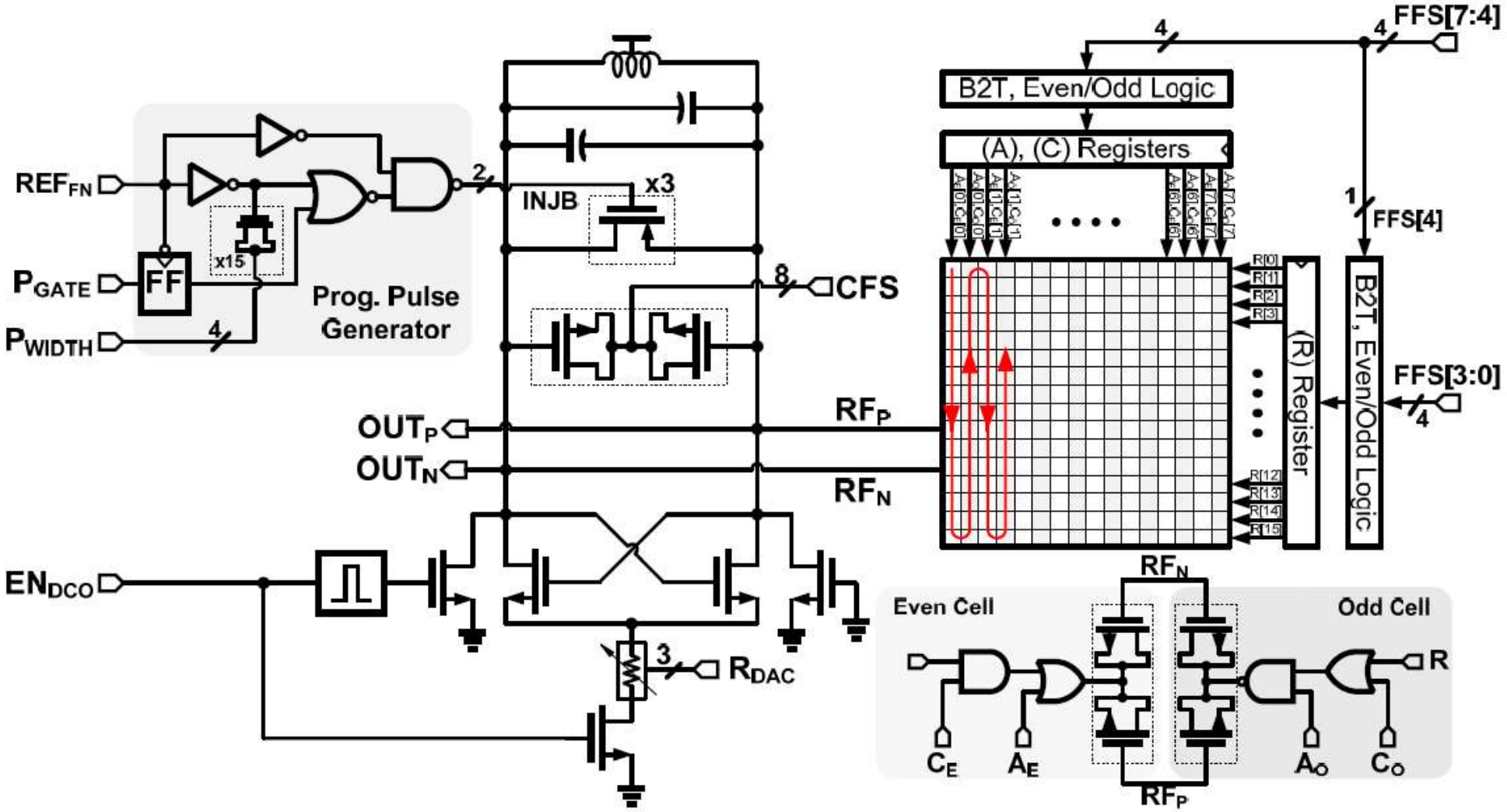
- **The most critical component**
- **Challenges**
  - Noise performance, PVT variation
  - Tuning range and the mechanism for tuning
- **2 main approaches**
  - Paring a DAC and a VCO
  - Digitally controlling a physical parameters





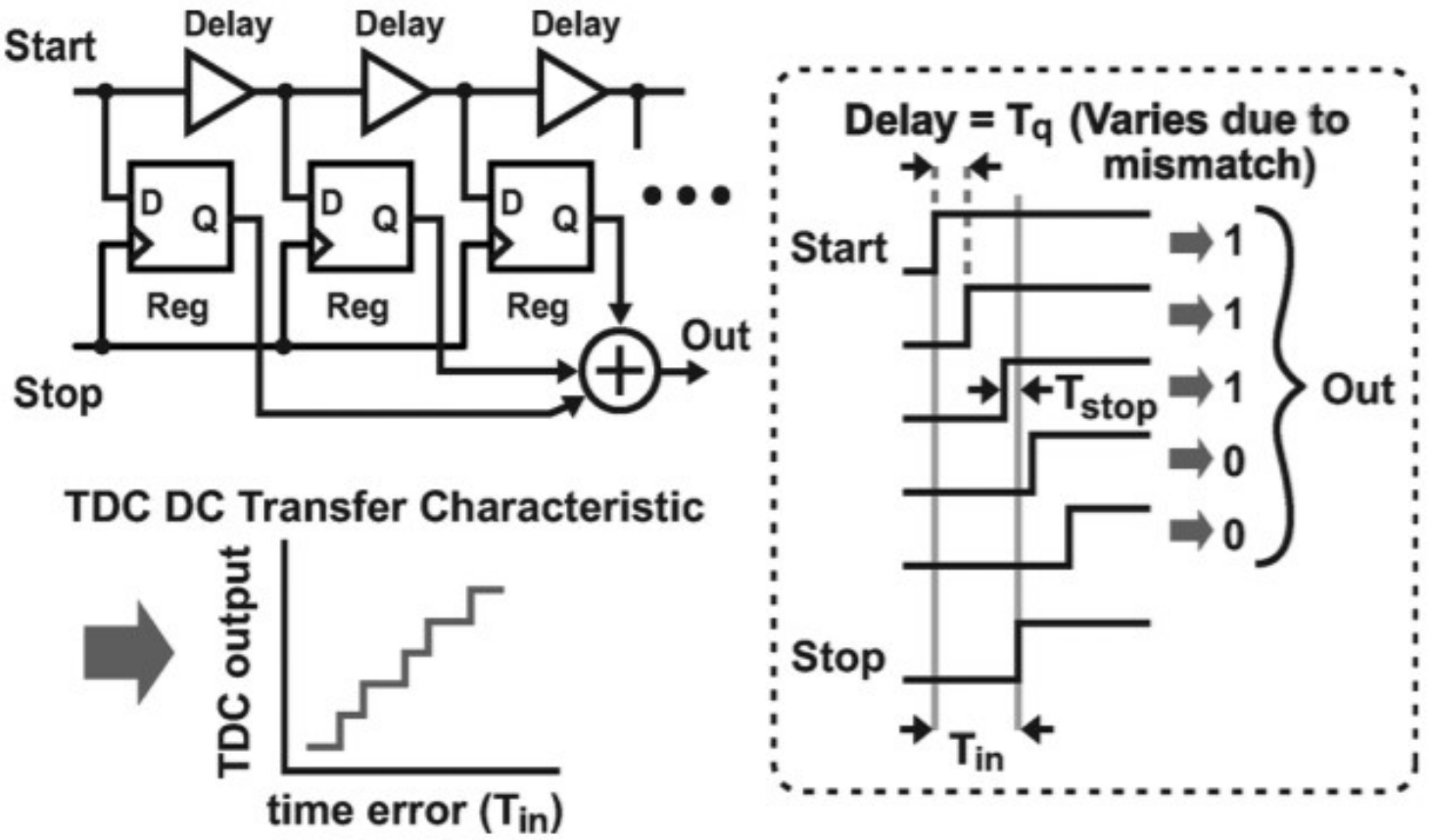
Injection-Locked 16b DCO

- ISSCC 2016, U. of Illinois & Xilinx



Conventional TDC

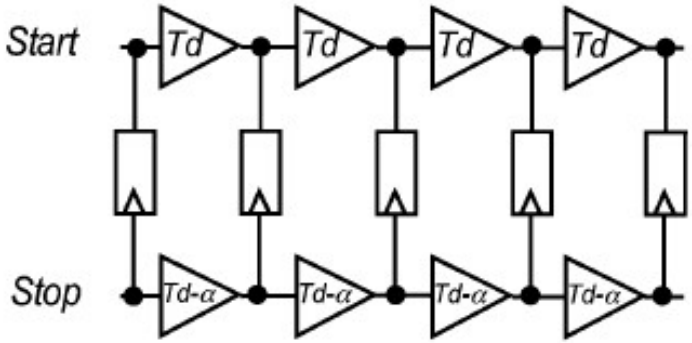
- Use linear delay element

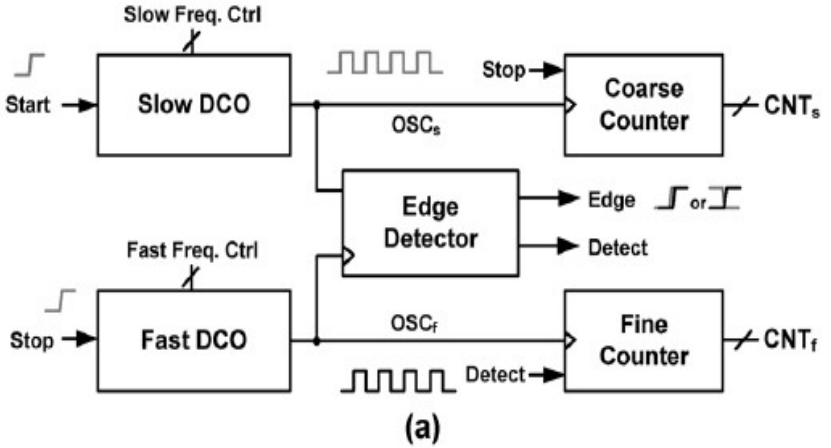


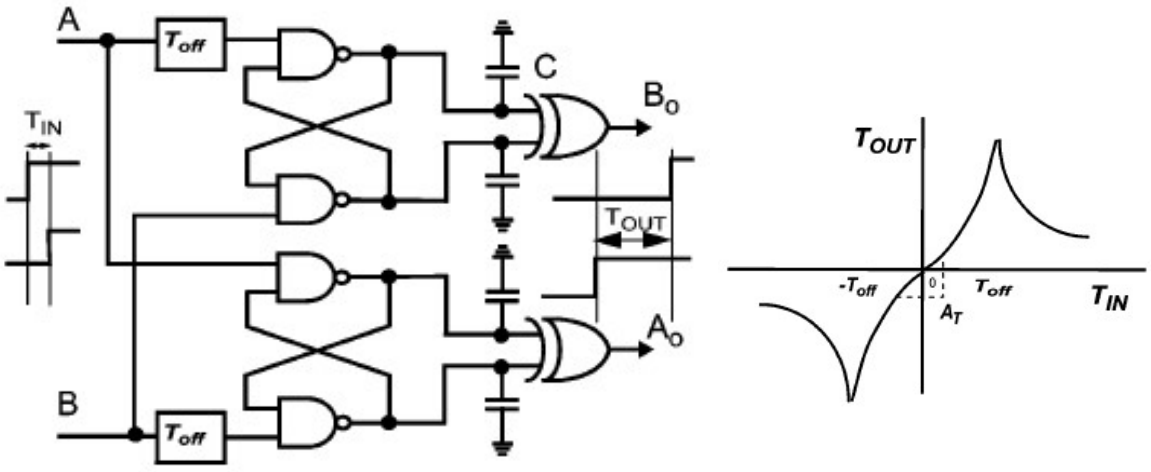
JSSC 2009

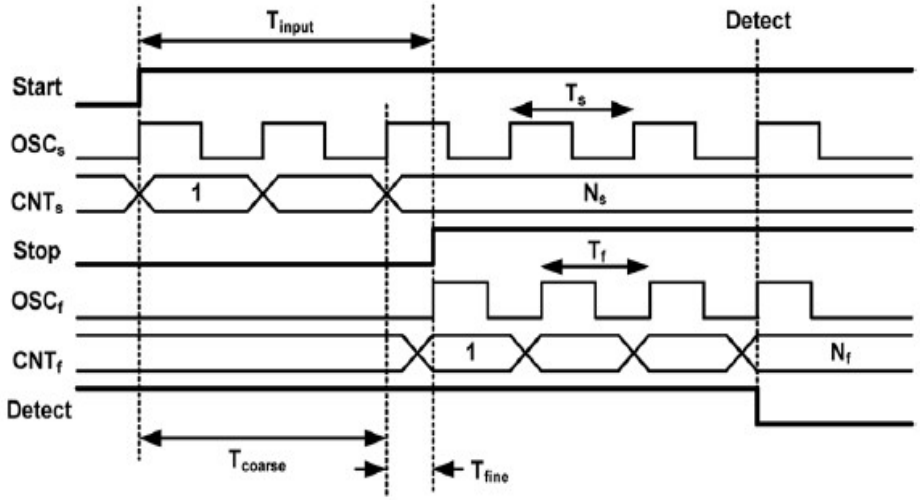
Improved TDC

- Vernier delay line, 2-stage with time-amplifier (2008 JSSC)
- Cyclic TDC (2011 JSSC)









CDR(Clock and Data Recovery)

- Needs
  - Optical communication
  - Backplane routing
  - Chip-to-chip interconnection
- Random data processing
  - Synchronous operation : data sensing
  - Receivers must generate clock : retimed
  - D-flipflop: data retiming, decision circuit
- Clock conditions
  - Frequency equal to the data
  - Phase relationship with respect to data
  - Small jitter

Simple CDR Circuit

- Structure
  - DFF as Phase Detector
  - Recovered clock ($Ck_{out} \leftarrow\rightarrow D_{in}$)
- Drawbacks
  - Full digital output PD
  - Large phase offset for data retiming (D-to-Q, CK-to-Q)
  - Feedthrough of data (to VCO output)
- PD needs skew avoiding
  - Sample the data by the clock

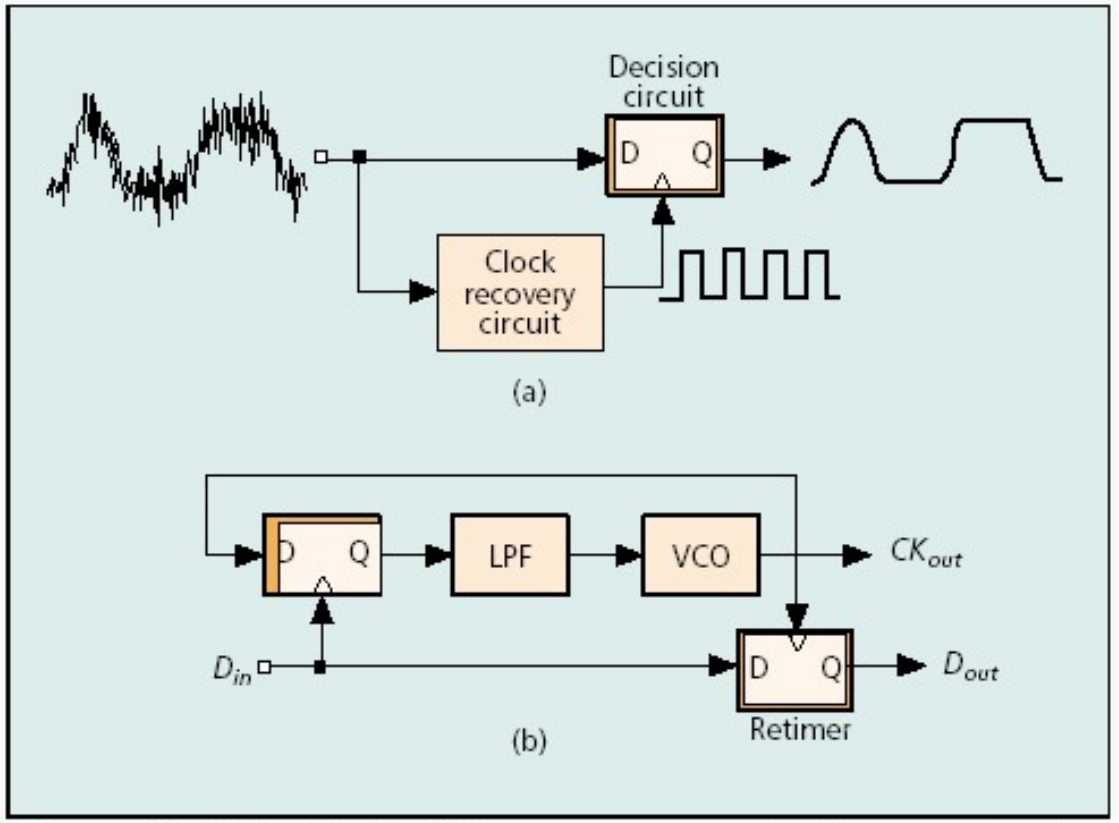


Figure 1. *a) The role of a CDR circuit in retiming data; b) an example of CDR implementation.*

IEEE spectrum

PLL Characteristics

- Specification & Performance
  - Frequency range
  - Loop Bandwidth
  - Jitter
    - cycle-to-cycle jitter, peak-to-peak jitter
    - histogram, eye-diagram, PPM
    - By thermal noise, supply noise and substrate noise
  - Lock time
  - Damping factor
  - Power consumption
  - Area
  - Synthesizable (for digital PLL)
  - Silicon proven (for Analog PLL)

Layout Issues

- Dummy layout
  - Density affects the characteristics of transistors
  - Dummy cell/pattern for low density portions
- Symmetry
  - Minimize process variation: VCO, …
  - Differential signal
- Separation
  - Geographical separation is best, guard
  - Substrate noise should be minimized: Substrate contacts, bypass C
- Supply
  - Different supply, independent supply for clock buffer
  - Capacitors between supply and ground
    → On-chip capacitor array, large capacitor is better
  - Use metal plane for supply

Other Considerations

- VCO
  - Guard
    - Every transistor : supply and ground
    - Every delay cell : ground guard
    - All VCO
  - Interconnection
    - The same line length and width
    - Elimination of 90 degree interconnection
  - Geography
    - The same cell direction(orientation) for every delay cell
    - Symmetrical cell layout
- ETC
  - ESD, Bias line routing, cross-talk
  - Stuffing option, corner simulation, di/dt, wire-to-wire C