Brief Papers

A Low-Swing Clock Double-Edge Triggered Flip-Flop

Chulwoo Kim, *Member, IEEE,* and Sung-Mo (Steve) Kang, *Fellow, IEEE*

***Abstract*—A low-swing clock double-edge triggered flip-flop (LSDFF) is developed to reduce power consumption significantly compared to conventional flip-flops. The LSDFF avoids unnecessary internal node transitions to reduce power consumption. In addition, power consumption in the clock tree is reduced because LSDFF uses a double-edge triggered operation as well as a low-swing clock. To prevent performance degradation of the LSDFF due to low-swing clock, low-V_t transistors are used for the clocked transistors without significant leakage current problems. The power saving in flip-flop operation is estimated to be 28.6% to 49.6% with additional 78% power saving in the clock network.**

I. Introduction

In many VLSI chips, the power dissipation of the clocking system, including clock distribution network and flip-flops, is often the largest portion of the total chip power consumption [1]–[3]. This is because the activity ratio of the clock signal is unity and the interconnect length of the clock trees has been increased significantly. The design trend is to use more pipeline stages for high throughput, which increases the number of flip-flops in a chip. Thus, it is important to reduce power consumption in both the clock trees and the flip-flops. Power consumption of a particular clocking scheme can be represented as

$$P_{\mathrm{ck-scheme}} = P_{\mathrm{ck-network}} + P_{\mathrm{FF}} \tag{1}$$

where $P_{\mathrm{ck-network}}$ and P_{FF} represent power consumptions in the clock network and flip-flops (FF), respectively. Each term in (1) can be expressed as

$$P_{\mathrm{ck-network}} = \left\{(C_{\mathrm{line}} + C_{\mathrm{ck-tr}}) \cdot V_{\mathrm{ck-swing}}^2\right\} \cdot f_{\mathrm{ck}} \tag{2}$$

$$P_{\mathrm{FF}} = \left\{(\alpha_{\mathrm{i}} \cdot C_{\mathrm{i}} \cdot \gamma + \alpha_{\mathrm{o}} \cdot C_{\mathrm{o}} \cdot \gamma + C_{\mathrm{ck-buf}}) \cdot V_{dd}^2\right\} \cdot f_{\mathrm{ck}} \tag{3}$$

where C_{line} is the interconnect line capacitance, $C_{\mathrm{ck-tr}}$ is the capacitance of the clocked transistors of the FF, C_{i} is the internal node capacitance of the FF, $C_{\mathrm{ck-buf}}$ is the capacitance of the clock buffers inside the FF, C_{o} is the output node capacitance of the FF, $V_{\mathrm{ck-swing}}$ is the clock swing voltage level, α_{i} is the internal node transition activity ratio, α_{o} is the output node transition activity ratio, and f_{ck} is the clock frequency. Also, γ is 2 for double-edge triggered FFs and 1 for single-edge triggered FFs.

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C. Kim was with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA. He is now with IBM Corporation, Austin, TX 78758 USA (e-mail: ckim5@us.ibm.com).

S.-M. Kang is with the Baskin School of Engineering, University of California, Santa Cruz, CA 95064 USA.

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To reduce power consumption in clock distribution networks, several small-swing clocking schemes have been proposed and their potential for practical applications has been shown [3], [4]. The previous half-swing scheme requires four clock signals. It suffers from skew problems among the four clock signals and requires additional chip area [4]. A reduced clock-swing flip-flop (RCSFF) requires an additional high power-supply voltage to reduce the leakage current [3]. A single-clock flip-flop for half-swing clocking does not need high power-supply voltage but has a long latency [2].

The hybrid-latch flip-flop (HLFF) and semidynamic flip-flop (SDFF) have been known as the fastest FFs, but they consume large amounts of power due to redundant transitions at internal nodes [5]–[7]. To reduce the redundant power consumption in internal nodes of high-performance flip-flops, the conditional capture flip-flop (CCFF) has been proposed [8]. However, HLFF, SDFF, and CCFF use full-swing clock signals that cause significant power consumption in the clock tree.

The rest of this paper is organized as follows. Section II describes the conventional flip-flops and their problems. In Sections III and V, we explain the proposed reduced swing single clock flip-flop and show simulation results of several flip-flops. Several power-saving approaches are compared in Section IV. In Section VI, we present a logic embedded flip-flop and its simulation results. Finally, conclusions are drawn in Section VII.

II. Conventional Flip-Flops

Fig. 1 shows several conventional small-swing clocking flip-flops. The half-swing flip-flop (HSFF) requires four clock signals, which suffers from skew problems among the four clock signals along with additional area, as shown in Fig. 1(a) and (b). Two upper swing clocks (CKP, CKPb) are fed to pMOS transistors and the other two lower swing clocks (CKN, CKNb) are fed to nMOS transistors. Hence, this scheme needs a special clock driver circuit that requires large capacitors. Also, this scheme increases the interconnect capacitance of clock networks and thus the power consumption. The speed degradation of the half-swing scheme also cannot be ignored. RCSFF uses only one clock signal, but it requires an additional high power-supply voltage for well bias control ($V_{\mathrm{well}} > V_{dd}$) to reduce the leakage current, as shown in Fig. 1(c). Although a simple clocking scheme can be used for RCSFF as shown in Fig. 1(d), its cross-coupled NAND gates form the speed bottleneck of RCSFF. Single clock flip-flop (SCFF) can operate with a half-swing clock because no pMOS transistors are driven by the clock, as shown in Fig. 1(e). It can also use a simple clocking scheme similar to Fig. 1(d). But the peak value of

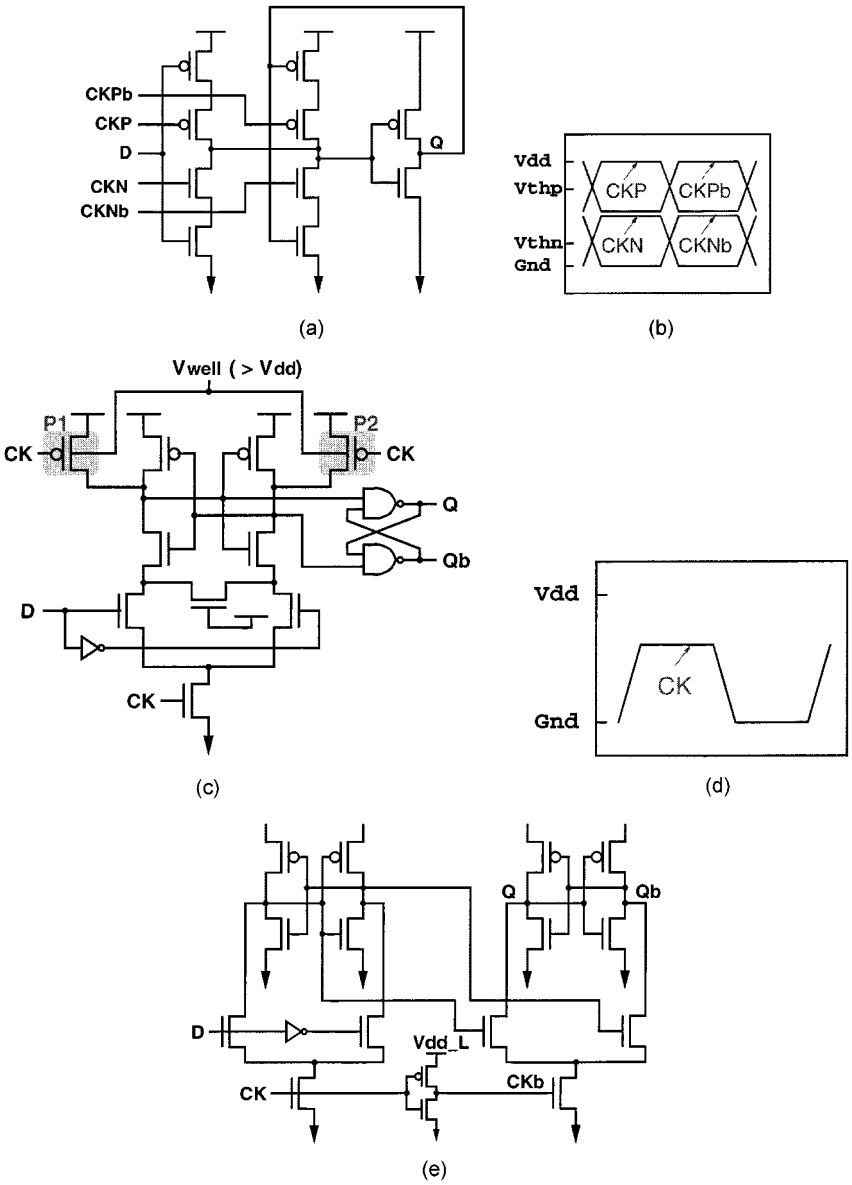

Fig. 1. Conventional small-swing clocking flip-flops. (a) HSFF. (b) Four clock signals for HSFF. (c) RCSFF. (d) Clock signal for RCSFF. (e) SCFF.

the clock signal in SCFF can be reduced to half V_{dd}. While its single clock phase is advantageous, a drawback of SCFF lies in its long latency; it samples data at the rising edge of the clock signal and transits sampled data at the falling edge of the clock signal. This long latency becomes a bottleneck for high-performance operation. SCFF also requires a second supply.

Both HLFF and SDFF, shown in Fig. 2(a) and (b), have been known as the fastest flip-flops, but they consume large amounts of power due to redundant transitions at internal nodes. CCFF has been proposed to reduce the redundant power consumption in internal nodes of high-performance flip-flops, as shown in Fig. 2(c) [8]. The conditional capture technique, however, needs many additional transistors for certain flip-flops such as SDFF, which tends to offset the power saving [9]. Furthermore, HLFF, SDFF, and CCFF use full-swing clock signals that cause significant power consumption in the clock tree.

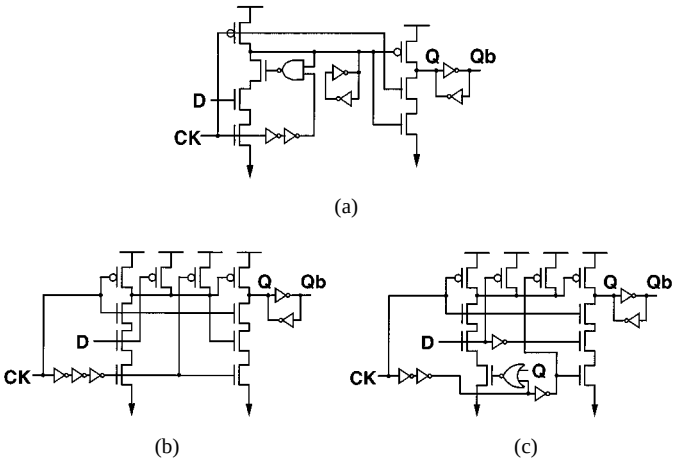

Fig. 2. Conventional high-performance flip-flops. (a) SDFF. (b) HLFF. (c) CCFF.

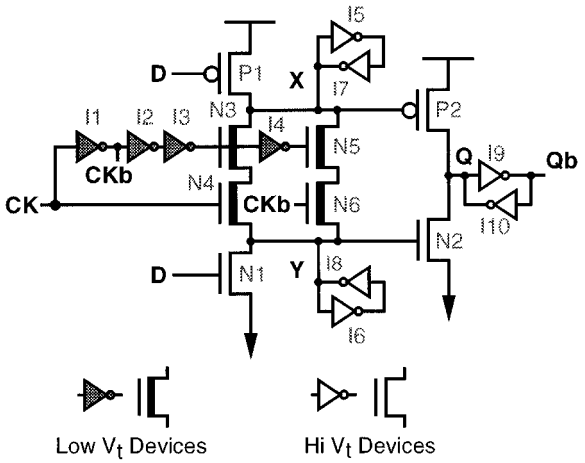

Fig. 3. Schematic of LSDFF.

III. Low-Swing Clock Double-Edge Triggered Flip-Flop

To overcome the problems of previous flip-flops, we propose a new low-swing clock double-edge triggered flip-flop (LSDFF). A schematic diagram of our LSDFF is shown in Fig. 3. It is composed of a data-sampling front end (P1, N1, N3–N6, I1–I4) and a data-transferring back end (P2, N2, I9, I10). I1–I4 are connected to a diode-connected nMOS transistor as a power source. Internal nodes X and Y are charged and discharged according to the input data D, not by the clock signal. Therefore, internal nodes of LSDFF switch only when the input changes. LSDFF does not require a conditional capture mechanism, as used in the pulse-triggered true-single-phase-clock (TSPC) flip-flop (PTTFF). In PTTFF, either one of the data-precharged internal nodes is in floating state, which may cause malfunction of the flip-flop. Also, its internal node does not have a full voltage swing, which causes performance degradation. To remove these shortcomings, two latches were introduced in LSDFF [10]. The use of one inverter and one transistor pairs (half-keeper) reduces fighting current, thus reducing the latency and power consumption. Although these latches improve performance, careful layout is required to minimize coupling noise. A noisy environment or clock gating operation may cause data loss of the LSDFF via coupling noise and/or leakage current through N3$\sim$ N6. A random input data transition can also cause data failure of LSDFF while not sampling. For such situations, back-to-back inverters (I5/I7 and I6/I8), instead of half-keepers, are recommended for robust operation of the LSDFF, as shown in Fig. 3, which may accompany a minor performance degradation. Avoidance of stacked transistors at the back end of the LSDFF further reduces the latency. Like HLFF, SDFF, and CCFF, a back-to-back-inverter type driver at the output node is used for robust operation.

The clock load in LSDFF is an nMOS transistor (N4) and an inverter (I1) and thus $C_{\mathrm{ck-tr}}$ in (3) is significantly reduced compared to previous FFs, as shown in Section V. Furthermore, the reduced clock swing ($V_{\mathrm{ck-swing}}$) technique can be easily applied without inducing static power dissipation or a complex clocking scheme. For the LSDFF, with a simple clocking scheme, double-edge triggering can be implemented to sample and transit data at both the rising edge and the falling edge of the clock. At the rising edge of the clock signal, transistor N3 and N4 are both turned on for the short duration of tp_1 to sample data, while at the falling edge of the clock signal, N5 and N6 are turned on to sample data during tp_2. Hence, the clock frequency f_{ck} in (2) can be lowered by half and accordingly, the clock network power consumption can be reduced by 50%. Fig. 4(a) shows the concept of the proposed clocking scheme and Fig. 4(b) shows equivalent implementation methods. With type A, timing skew between CKd and CKdb can be minimized by tuning the transistor sizes of inverters. For type B, a pulsed-clock signal can be generated from an additional pulsed-clock generator. Although the inverter overhead is removed in the LSDFF, degradation of the pulse amplitude and width may be a problem for clock signal propagation. Type C is considered the best for removing timing skew with some additional power consumption.

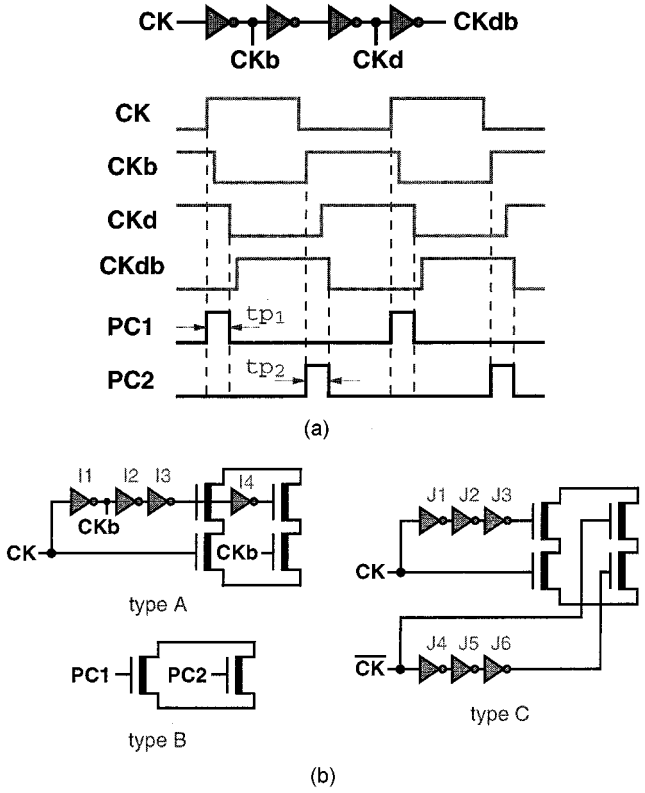

Fig. 4. (a) Clock timing diagram for LSDFF. (b) Three short pulse-clock generation methods.

The operation of the LSDFF is explained next. Referring to Fig. 3, prior to the rising edge of clock signal CK, N3$\sim$ N6 are off. When the input changes to "Hi," node Y is discharged to "Lo" through nMOS transistor N1 and node X retains the previous data value. After the rising edge of CK, N3 and N4 are on and node X is discharged to (or kept) "Lo" according to the previous status. This node X drives the gate of P2, which in turn charges the output node Q to "Hi." When the input changes to "Lo," node X is charged to "Hi" through pMOS transistor P1 and node Y retains the previous data value "Lo." After the rising edge of CK, N3 and N4 are on and node Y is charged to $V_{dd}-V_{\mathrm{th-N3}}$ and finally to V_{dd} by P3. Node Y drives the gate of N2 and N2 discharges the output node Q to "Lo." The operation at the falling edge of CK can be explained in a similar manner.

TABLE I
COMPARISON OF POWER SAVING APPROACHES

	$P_{ck-network}$			P_{FF}	
	C_{ck-tr}	$V^2_{ck-swing}$	f_{ck}	α_i	$C_{ck-buf} \cdot f_{ck}$
CCFF				√	
RCSFF	√	√			
LSDFF	√	√	√	√	√

To prevent performance degradation of the LSDFF due to reduced clock swing, low-V_t transistors ($|V_{t-low}| = 0.15$ V) are used for the clocked transistors (N3–N6). Subthreshold current flow of low-V_t devices will be significant in very deep submicron (VDSM) technology and should be controlled to reduce the leakage power consumption. In the LSDFF, the leakage current of transistors N3–N6 will be limited by a turned-off high-V_t transistor, either P1 or N1 according to input data D ($|V_{t-hi}| = 0.38$ V). For propagation of reduced clock-swing signals, inverters with low-V_t transistors (I1–I3) can be used along with a low power-supply voltage which was generated from high supply voltage with a diode-connected nMOS transistor. Leakage currents of these inverters are not significant for low power-supply voltage.

IV. COMPARISON OF POWER-SAVING APPROACHES

We have described power-saving approaches of several conventional flip-flops and the proposed LSDFF in the previous sections. In this section, we will summarize different approaches to reducing the power consumption of the clocking scheme. First, CCFF reduces the power consumption of HLFF by removing redundant internal data holding node switching, thus reducing α_i in (3). Second, small-swing clock flip-flops (HSFF, RCSFF, and SCFF) reduce power consumption in the clock network by reducing the clock voltage swing. Also, the capacitance of clocked transistors of the FF, C_{ck-tr}, in (2) is also reduced in RCSFF. Finally, LSDFF uses both a low-swing clock and a double-edge triggered operation to reduce power consumption in the clock network. Further, LSDFF does not have any redundant internal data holding node switching. Table I summarizes power-saving approaches in each flip-flop.

V. EXPERIMENTAL RESULTS COMPARISON

We have analyzed several conventional flip-flops and have developed a new flip-flop in a 0.18-μm CMOS process. Each flip-flop is optimized for power-delay product. The simulation conditions were 1.5 V V_{dd} and 80 °C with the clock frequency at 125 MHz for LSDFF and 250 MHz for conventional single-edge triggered FFs to achieve the same throughput. The low-swing clock voltage for LSDFF was about 1 V. The output load capacitance was assumed to be 100 fF. The simulated waveforms of the LSDFF are shown in Fig. 5. Comparisons of simulation results for the four FFs are summarized in Table II. As Fig. 6 shows, LSDFF has the least power consumption when the input pattern does not change, whereas HLFF and SDFF still incur high power consumption even though the input stays 1. For an average input switching activity of 0.3, the power consumption of LSDFF is reduced by 28.6% ∼ 49.6% over conventional FFs, as

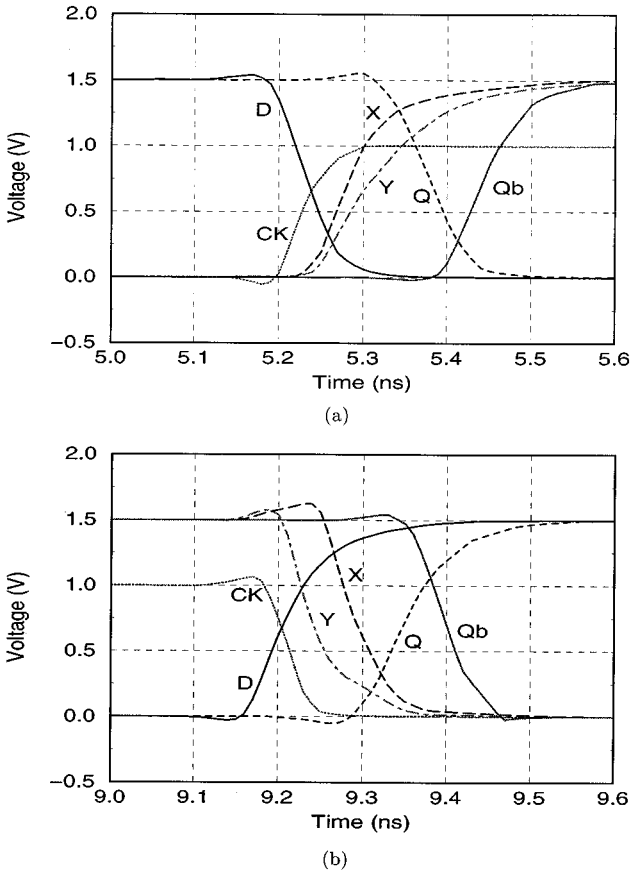

Fig. 5. Simulated waveforms. (a) "Hi" to "Lo" transition of Q at rising edge of the clock. (b) "Lo" to "Hi" transition of Q at falling edge of the clock.

TABLE II
COMPARISONS OF FLIP-FLOPS

	No. of Tr.	No. of clked Tr.	Ck-$\bar{Q}$ (ps)	min. D-$\bar{Q}$ (ps)	Power (uW)	P·D (fJ)
SDFF	23	5	175	178	262	46.6
HLFF	20	4	185	190	250	47.5
CCFF	26	5	184	188	185	34.8
LSDFF	28	3	194	199	132	26.3

shown in Fig. 6, mainly due to halved clock frequency and elimination of unnecessary internal node transitions. Power-delay product is also reduced by 28.7% ∼ 47.8% with comparable D-to-$\bar{Q}$ delay. The Clk-to-$\bar{Q}$ delay comparisons are not suitable for a relevant performance parameter because they do not consider the setup time and, therefore, the effective time taken out of the clock cycle [7]. Hence, we used the D-to-$\bar{Q}$ delay as the delay parameter of a flip-flop. The optimum setup time of LSDFF is measured based on the methodology in [7] and is negative (−35 ps), which is an important attribute of soft-clock edge for time borrowing and for overcoming clock-skew problems. As shown in Fig. 7, an additional 78% power savings in clock network can be achieved by the reduced clock-swing scheme and 50% reduction in clock frequency.

VI. EMBEDDED LOGIC IN LSDFF

Simple logic elements can be embedded into LSDFF to reduce overall delays within a pipeline stage. With embedded

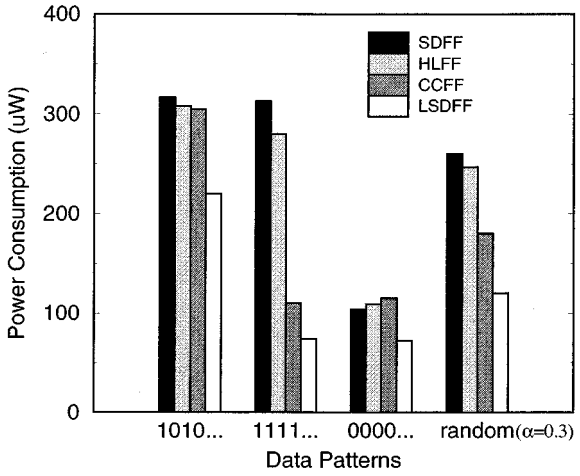

Fig. 6. Flip-flop power consumption comparisons dependent on data patterns.

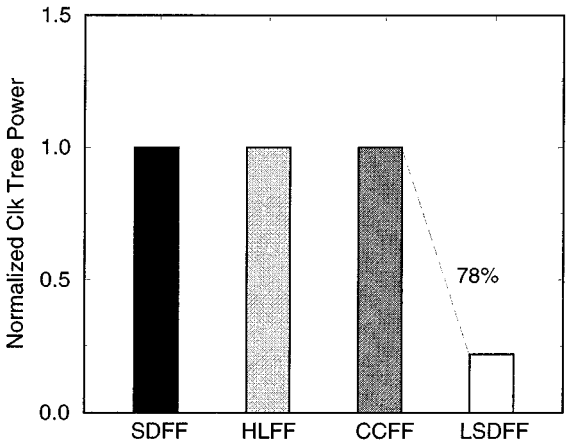

Fig. 7. Normalized clock network power consumption comparisons.

TABLE III
SPEED COMPARISONS OF LSDFF WITH EMBEDDED LOGIC VERSUS DISCRETE LOGIC

	D	A·B	A+B	A·B+C·D
Embedded	199ps	219ps	229ps	246ps
Discrete	199ps	298ps	305ps	367ps
Speedup	1.0	**1.36**	**1.33**	**1.49**

logic in LSDFF, the overall circuit performance can be optimized by saving a gate in critical paths. Table III shows that the speedup factor of embedded logic in LSDFF over discrete logic ranges from 1.33 to 1.49.

VII. CONCLUSION

A low-swing clock double-edge triggered flip-flop (LSDFF) has been developed in a 0.18-μm dual-V_t CMOS process to reduce power consumption in both the clock trees and the flip-flops. The LSDFF inherently avoids unnecessary internal node transitions. Furthermore, LSDFF uses a double-edge triggered operation as well as a low-swing clock, which reduces power consumption in the clock tree. The overall power saving of LSDFF is significant over conventional high-performance flip-flops with comparable D-to-$\bar{Q}$ delay. Also, an additional 78% power saving is achieved in the clock network. For robust operation, back-to-back inverters instead of IN5/N7 and I6/P3 can be used to hold the data of internal nodes. The negative setup time of LSDFF helps to overcome the clock skew problems. With simple logic embedding, LSDFF reduces overall delays within a pipeline stage.

REFERENCES

[1] H. B. Bakoglu, *Circuits, Interconnections and Packaging for VLSI*. New York: Addison Wesley, 1990.
[2] Y.-S. Kwon, I.-C. Park, and C.-M. Kyung, "A new single clock flip-flop for half-swing clocking," *IEICE Trans. Fundamentals*, vol. E82-A, no. 11, pp. 2521–2526, Nov. 1999.
[3] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% clock power reduction," *IEEE J. Solid-State Circuits*, vol. 33, pp. 807–811, May 1998.
[4] H. Kojima, S. Tanaka, and K. Sasaki, "Half-swing clocking scheme for 75% power saving in clocking circuitry," *IEEE J. Solid-State Circuits*, vol. 30, pp. 432–435, Apr. 1995.
[5] E. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in *IEEE Int. Solid-State Circuits Conf.*, Feb. 1996, pp. 138–139.
[6] F. Klass, "Semi-dynamic and dynamic flip-flops with embedded logic," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1998, pp. 108–109.
[7] V. Stojanovic and V. G. Oklobdzija, "Comparative analysis of master–slave latches and flip-flops for high-performance and low-power systems," *IEEE J. Solid-State Circuits*, vol. 34, pp. 536–548, Apr. 1999.
[8] B. Kong, S.-S. Kim, and Y.-H. Jun, "Conditional-capture flip-flop technique for statistical power reduction," in *IEEE Int. Solid-State Circuits Conf.*, Feb. 2000, pp. 290–291.
[9] M. Hamada, T. Terazawa, T. Higashi, S. Kitabayashi, S. Mita, Y. Watanabe, M. Ashino, H. Hara, and T. Kuroda, "Flip-flop selection technique for power-delay trade-off," in *IEEE Int. Solid-State Circuits Conf.*, Feb. 1999, pp. 270–271.
[10] C. Kim and S.-M. Kang, "A low-swing clock double edge-triggered flip-flop," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 2001, pp. 183–186.