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Nanoscale MOSFET Modeling

Part 1: The simplified EKV model for the design of low-power analog circuits

This article presents the simplified charge-based Enz–Krummenacher–Vittoz (EKV) [11] metal–oxide–semiconductor field-effect transistor (MOSFET) model and shows that it can be used for advanced complementary metal–oxide–semiconductor (CMOS) processes despite its very few parameters. The concept of an inversion coefficient (IC) is first introduced as an essential design parameter that replaces the overdrive voltage $V_G - V_{T0}$ and spans the entire range of operating points from weak via moderate to strong inversion (SI), including the effect of velocity saturation (VS). The simplified model in saturation is then presented and validated for different 40- and 28-nm bulk CMOS processes. A very simple expression of the normalized transconductance in saturation, valid from weak to SI and requiring only the VS parameter λ_c, is described. The normalized transconductance efficiency G_m/I_D, which is a key figure-of-merit (FoM) for the design of low-power analog circuits, is then derived as a function of IC including the effect of VS. It is then successfully validated from weak to SI with data measured on a 40-nm and two 28-nm bulk CMOS processes. It is then shown that the normalized output conductance G_{ds}/I_D follows a similar dependence with IC than the normalized G_m/I_D characteristic but with different parameters accounting for drain induced barrier lowering (DIBL). The methodology for extracting the few parameters from the measured $I_D - V_G$ and $I_D - V_D$ characteristics is then detailed. Finally, it is shown that the simplified EKV model can also be used for a fully depleted silicon on insulator (FDSOI) and FinFET 28-nm processes.

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Introduction

With its stringent requirements on the energy consumption of electronic

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devices, the Internet of Things has become the primary driver for the design of low-power analog and radio-frequency (RF) circuits [1]. The implementation of increasingly complex functions under highly constrained power and area budgets, while circumventing the challenges posed by modern device technologies, makes the analog/RF design exercise ever more challenging. The designer often needs to make optimum choices to achieve the required gain, current efficiency, bandwidth, linearity, and noise performance [2], [3].

To this purpose, he often starts his new design using simple transistor models to explore the design space and identify the region offering the best tradeoff before fine-tuning his design by running more accurate simulations using the full fetched compact model available in the design kit [4], [5]. This task has been made more difficult in advanced CMOS technologies due to the down-scaling of CMOS processes and the reduction of the supply voltage, which has progressively pushed the operating point from the traditional SI region toward moderate (MI) and even weak inversion (WI), where the simple quadratic model is obviously no more valid [6], [7]. This has led to an increased interest in the concept of *IC* as the main design parameter replacing the overdrive voltage even for advanced technologies [8], [9].

This article presents the simplified EKV transistor model in saturation since, except for switches, most transistors in CMOS analog circuits are biased in saturation. The article is split in two parts: the first part introduces the simplified EKV model in saturation and shows that it can be used even for advanced bulk CMOS technologies. The second part of the article, to be published in an upcoming issue of *IEEE Solid-State Circuits Magazine*, will show how the inversion coefficient can be used as the main design parameter to describe various FoMs to explore basic tradeoffs faced in analog and RF design.

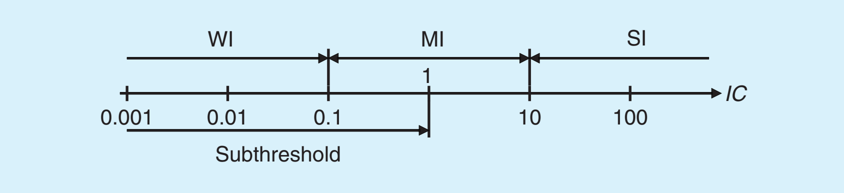

FIGURE 1: The different regions of operation in terms of the inversion coefficient.

The Concept of Inversion Coefficient

Definition

The *inversion coefficient IC* is a measure of the inversion level in the channel of a single MOSFET and is defined as [10]

$$IC \triangleq \frac{I_D}{I_{spec}}\Big|_{\text{saturation}}, \quad (1)$$

where the normalizing factor I_{spec} is called the *specific current* and is defined as [10]

$$I_{spec} \triangleq I_{spec\square} \cdot \frac{W}{L} \quad \text{with}$$
$$I_{spec\square} \triangleq 2n\mu_0 C_{ox} U_T^2, \quad (2)$$

where W and L are the width and length of the transistor, n is the slope factor, μ_0 is the low field mobility in the channel region, C_{ox} the oxide capacitance per unit area, and $U_T \triangleq kT/q$ is the thermodynamic voltage. In a given technology, the specific currents per square $I_{spec\square}$, one for each transistor type (n- and p-channel), are the most fundamental parameters for the designer.

Using IC, the different regions of operation of a MOSFET can be classified as illustrated in Figure 1 and defined as

$$\begin{aligned} &IC \le 0.1 \text{ WI}, \\ &0.1 < IC \le 10 \text{ MI}, \\ &10 < IC \text{ SI}. \end{aligned} \quad (3)$$

The specific current has originally been defined in [11] using the normalized $G_m n U_T / I_D$ characteristic as discussed in the section "The Transconductance Efficiency G_m/I_D." It corresponds to the drain current for which the long-channel SI asymptote $1/\sqrt{IC}$ crosses the WI asymptote, which turns out to be equal to unity as shown in Figure 2.

The specific current I_{spec} can actually be extracted for a given technology and transistor type using the circuit shown in Figure 3 [12], [13]. This circuit is based on the Vittoz current reference represented by transistors M1–M4, where the original resistor is replaced by M6 [14]. M1 and M2 are biased in WI and saturation, whereas M6 and M7 in SI (M6 in the linear region and M7 in saturation). Assuming that $A \gg 1$, it

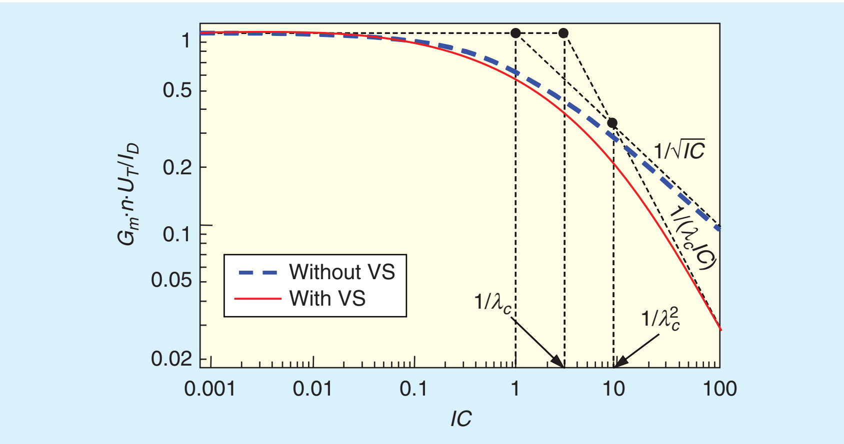

FIGURE 2: g_{ms}/i_d versus IC showing the long- and short-channel asymptotes.

The designer often needs to make optimum choices to achieve the required gain, current efficiency, bandwidth, linearity, and noise performance.

can be shown that the bias current I_b is proportional to I_{spec6} and I_{spec7}

$$I_b = I_{spec6} \cdot A \cdot ln^2(K) = I_{spec7} \cdot ln^2(K), \quad (4)$$

where $K \triangleq \beta_2/\beta_1$ with $\beta_i = \mu_0 C_{ox} W_i/L_i$ for $i = 1, 2$. This circuit allows the inversion coefficient of any n-channel transistor to be precisely set independently of the value of the threshold voltage from the reference transistor. Indeed, any n-channel transistor Mx can be operated at a given inversion factor IC_x by means of a weighted copy of current I_b. For a transistor Mx that has to be biased in WI, it is best to use transistor M1 as a reference transistor whereas M7 should be used as reference transistor for biasing a transistor in SI. The drain current of transistor Mx is then N times the bias current $I_x = N \cdot I_b$ and hence $IC_x \cdot W_x/L_x = N \cdot IC_1 \cdot W_1/L_1$. The aspect ratio W_x/L_x of transistor Mx is then given by

$$\frac{W_x}{L_x} = N \cdot \frac{IC_1}{IC_x} \cdot \frac{W_1}{L_1}. \quad (5)$$

This circuit is therefore ideal for migrating circuits from one technology to another with a minimum of redesign. Note that another current reference is needed for extracting the specific current for p-channel transistors.

The Simplified EKV MOSFET Model

The Large-Signal dc Model

The drain current in saturation normalized to the specific current, which actually corresponds to IC defined earlier, is given by [15], [16]

$$IC = \frac{4(q_s^2 + q_s)}{2 + \lambda_c + \sqrt{4(1+\lambda_c) + \lambda_c^2 (1 + 2q_s)^2}}, \quad (6)$$

where q_s is the normalized inversion charge $q_i \triangleq Q_i/Q_{spec}$ taken at the source with $Q_{spec} \triangleq -2nU_T C_{ox}$ [10]. Parameter λ_c is accounting for VS according to

$$\lambda_c \triangleq \frac{L_{sat}}{L} \quad (7)$$

and scales inversely proportional to the transistor length L. λ_c actually corresponds to the fraction of the channel in which the carrier drift velocity reaches the saturated velocity v_{sat} over a portion of the channel length L_{sat} defined as

$$L_{sat} = \frac{2\mu_0 U_T}{v_{sat}}. \quad (8)$$

The normalized source charge q_s is related to the terminal voltages by [10]

$$\frac{V_P - V_S}{U_T} = 2q_s + ln(q_s), \quad (9)$$

where $V_P - V_S$ is the saturation voltage for a long-channel transistor (i.e., without VS), $V_P \cong (V_G - V_{T0})/n$ is the pinch-off voltage, and V_S is the source-to-bulk voltage. Note that, in the EKV model, all the terminal voltages are referred to the local substrate instead of the source terminal to preserve the symmetry of the device in the model [10].

The normalized saturation voltage can be expressed in terms of the inversion coefficient IC by solving (6) for q_s leading to

$$q_s = \frac{1}{2} \cdot \left(\sqrt{4IC + (1 + \lambda_c \cdot IC)^2} - 1\right) \quad (10)$$

and using (10) in (9). Unfortunately, (9) cannot be inverted to express IC in terms of $V_P - V_S$ and hence of the terminal voltages.

This simplified charge-based model only requires four parameters to fit the $I_D - V_G$ transfer characteristic: the slope factor n, the specific current per square $I_{spec\square}$, the threshold voltage V_{T0}, and the VS parameter L_{sat}. The methodology to extract these parameters from measured data is explained in the section "Parameter Extraction." Typical values for these parameters for a 28-nm bulk CMOS process are given in Table 1.

The I_D versus $V_G - V_{T0}$ transfer characteristics are plotted in Figure 4

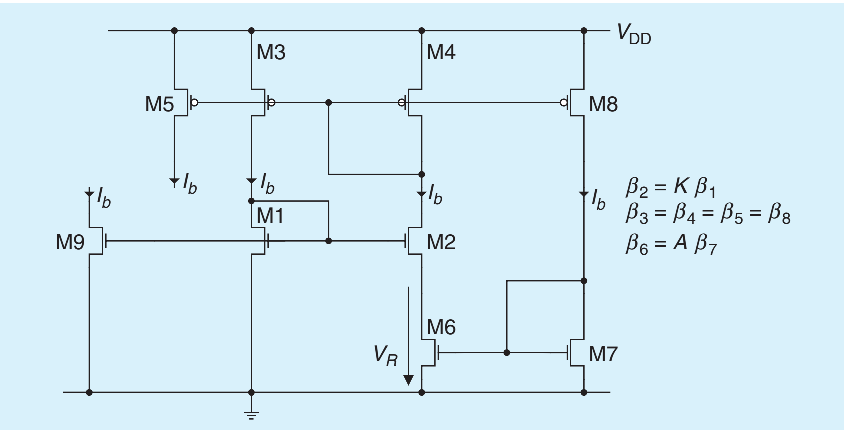

FIGURE 3: The current reference for extracting the specific current for n-channel transistors [12]–[14].

TABLE 1. TYPICAL PARAMETER VALUES FOR A 28-nm PROCESS.

	n	$I_{spec\square}$ [nA]	V_{T0} [V]	L_{sat} [nm]
n-channel	1.1–1.5	850	0.4–0.55	15–25
p-channel	1.1–1.5	350	0.35–0.5	15–25

and compared to measurements made on wide and minimal length transistors from three different processes, a 40-nm and two different 28-nm bulk CMOS processes. Although the drain current is measured from sweeping the gate voltage, the simplified EKV model is calculated from the measured current by first normalizing it to the specific current for each transistor to get the inversion coefficients, from which the overdrive voltages are computed using (10) and (9). Despite the very few number of parameters, the simple model fits the measurements very well over more than six decades of current. Note that the extraction of the parameters $I_{spec□}$ and L_{sat} is done for several different geometries (in particular, different length) illustrating the rather good scalability of the simplified model. Notice that the measured points and analytical models of the $W = 108\,\mu m, L = 30\,nm$ (red circles) and $W = 108\,\mu m, L = 40\,nm$ (green squares) transistors almost fall on top of each other, indicating that the normalization almost completely strips off the technology dependence. The difference with the $W = 3\,\mu m, L = 30\,nm$ (blue diamonds) characteristic is due to a slightly larger value of λ_c. In other words, the four parameters almost fully characterize the technology at least for the transfer characteristics in saturation and in the regions of operation used for analog circuit design.

The large-signal output characteristic in the saturation region has always been the most difficult part to model due to a combination of several effects including VS, channel length modulation (CLM) and DIBL. Figure 5 shows the inversion coefficient versus the drain voltage for different overdrive voltages measured on a large and minimal length transistor from a 28-nm process. It shows that the current can be approximated in saturation by a simple linear characteristics

$$I_D \cong G_{ds} \cdot (V_D + V_M), \qquad (11)$$

where V_M is the CLM (or Early) voltage and G_{ds} is the output conductance that corresponds to the slope and is discussed further in the next section. (Note that even though the parameter V_M is called the CLM voltage, it actually embeds all of the effects, including VS and DIBL, which is actually dominant in WI.)

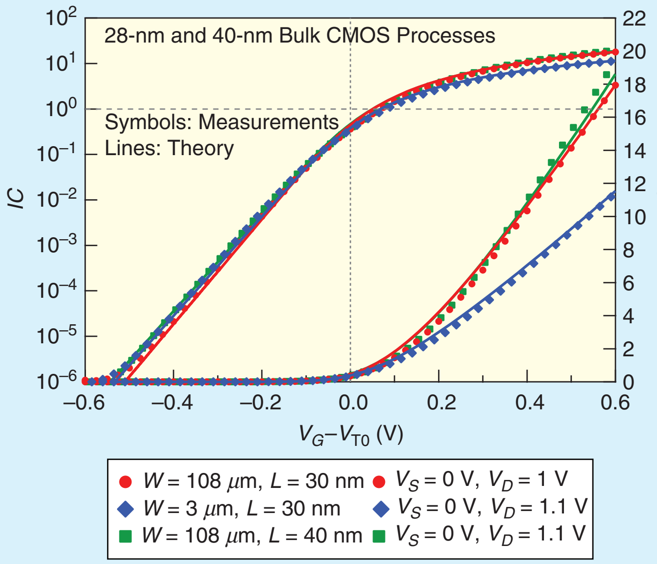

FIGURE 4: *IC* versus the overdrive voltage $V_G - V_{T0}$ measured in saturation on minimum length transistors from a 40-nm and two different 28-nm bulk CMOS processes.

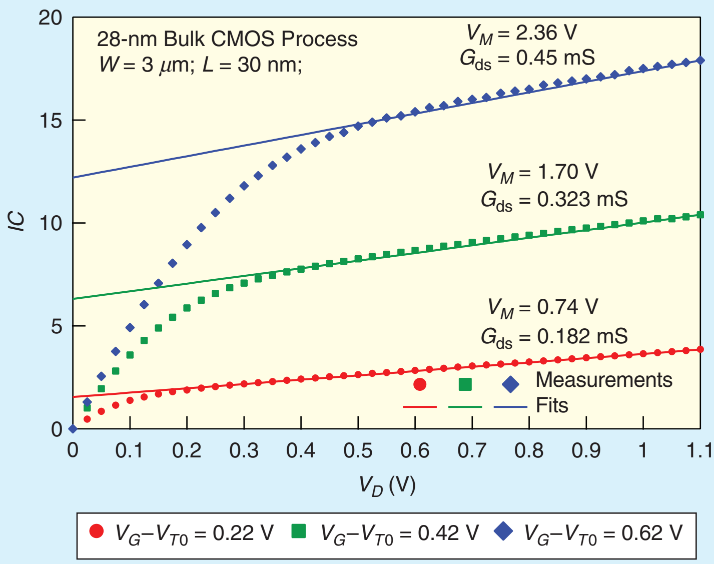

FIGURE 5: *IC* versus V_D measured for different overdrive voltages on a minimum length transistor 30-nm from a 28-nm bulk CMOS processes.

The Small-Signal dc Model

The most important small-signal parameter is without doubt the gate transconductance G_m. Since in the EKV model the voltages are all referred to the bulk, we can define two other transconductances: the source transconductance $G_{ms} \triangleq -\partial I_D/\partial V_S$ and the drain transconductance $G_{md} \triangleq \partial I_D/\partial V_D$ [10]. Note that G_{md} should not be confused with the output conductance G_{ds}. In saturation $G_{md} = 0$ and $G_{ms} = n \cdot G_m$.

The transconductance efficiency, sometimes also called the current efficiency, is one of the most important FoMs for low-power analog circuit design.

The normalized source transconductance in saturation g_{ms} can be expressed in terms of IC as [4], [15]

$$g_{ms} \triangleq \frac{G_{ms}}{G_{spec}} = \frac{n \cdot G_m}{G_{spec}} = \frac{\sqrt{(\lambda_c IC + 1)^2 + 4IC} - 1}{\lambda_c(\lambda_c IC + 1) + 2}, \quad (12)$$

where $G_{spec} \triangleq I_{spec}/U_T = 2n\mu_0 C_{ox} U_T$. g_{ms} is plotted versus IC in Figure 6 and favorably compares to measurements obtained from the derivative of the characteristics shown in Figure 4 over a very wide range of bias (more than four decades of current). Note that for short-channel devices in SI, the $I_D - V_G$ transfer characteristic becomes a linear function of the gate voltage as illustrated in Figure 4 and, hence, the gate transconductance becomes independent of the drain current and of the gate length L. It then only depends on W and v_{sat} according to

$$g_{ms} \cong 1/\lambda_c \text{ for } IC \gg 1 \quad \text{or} \quad G_m \cong W C_{ox} v_{sat}. \quad (13)$$

The inverse of the VS parameter λ_c is therefore a key parameter since it gives the maximum normalized transconductance that can be achieved for a short-channel device in a given technology.

The other key dc small-signal parameter is the output conductance G_{ds} which, together with the transconductance, defines the intrinsic (or self) gain G_m/G_{ds}. As mentioned previously, the output conductance is the result of several physical effects including VS, CLM, and DIBL. In advanced short-channel devices biased in MI or WI, DIBL is the dominant effect. The latter is defined as the variation of the threshold voltage with respect to the applied drain-to-source voltage, i.e., $\partial V_T/\partial V_{DS}$ and can be modeled as [17]–[19]

$$V_T \cong V_{T0} \cdot (1 - \sigma_d \cdot V_{DS}), \quad (14)$$

where the parameter $\sigma_d \triangleq \partial V_T/\partial V_{DS}$ accounts for DIBL and depends on L and V_S [18], [19]. The output conductance can then be written as [20]

$$G_{ds} \triangleq \frac{\partial I_D}{\partial V_{DS}} = \frac{\partial I_D}{\partial V_T} \cdot \frac{\partial V_T}{\partial V_{DS}} = \sigma_d \cdot G_m, \quad (15)$$

where $\partial I_D/\partial V_T = -G_m$ has been used. A model of the output conductance versus IC can now be derived using the expression of $G_m = G_{ms}/n$ in saturation given in (12), where λ_c is replaced by an additional parameter λ_d

$$g_{ds} \triangleq \frac{G_{ds}}{G_{spec}} = \frac{\sigma_d}{n} \cdot \frac{\sqrt{(\lambda_d IC + 1)^2 + 4IC} - 1}{\lambda_d(\lambda_d IC + 1) + 2}. \quad (16)$$

The normalized output conductance versus IC given by (16) is plotted in Figure 7 and compared to measurements made on a long and short transistor from a 28-nm CMOS process. Figure 7 shows that the model fits very well the measured data over more than five decades of current despite its simplicity.

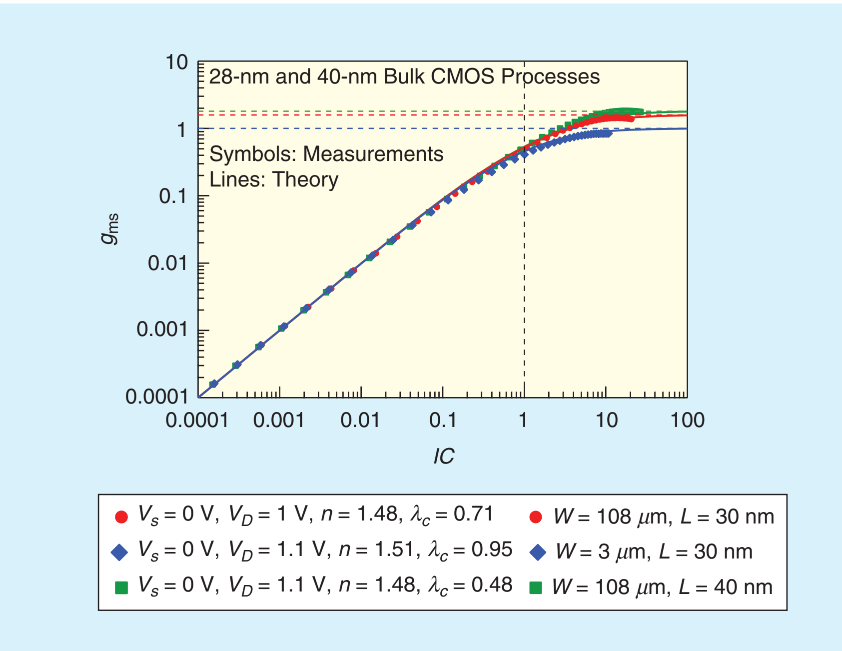

FIGURE 6: Normalized transconductance g_{ms} versus IC measured on minimum length transistors from a 40-nm and two different 28-nm bulk CMOS processes.

The Transconductance Efficiency G_m/I_D

The transconductance efficiency G_m/I_D, sometimes also called the *current efficiency*, is one of the most important FoMs for low-power analog circuit design. It is a measure of how much transconductance is produced for a given bias current and is a function of IC. As will be shown in the second part of this article, the transconductance efficiency (or its inverse) appears in many expressions related to the optimization of analog circuits. In normalized form, the transconductance efficiency is defined as the actual transconductance obtained at a given IC with respect to the maximum transconductance $G_m = I_D/(nU_T)$ reached in WI [4], [15]

$$\frac{g_{ms}}{IC} = \frac{G_m \cdot nU_T}{I_D} = \frac{\sqrt{(\lambda_c IC + 1)^2 + 4IC} - 1}{IC \cdot [\lambda_c(\lambda_c IC + 1) + 2]}. \quad (17)$$

The expression in (17), which is continuous from WI to SI and includes the effect of VS, is plotted in Figure 2. The figure shows that $G_m n U_T / I_D$ is maximum in WI and decreases as $1/\sqrt{IC}$ in SI for long-channel devices in which VS is absent (dashed blue curve). Note that the specific current has been defined from the $G_m n U_T / I_D$ versus I_D characteristic of a long-channel transistor as the current at which the WI and SI asymptotes cross. This is why these two asymptotes cross at $IC = 1$ when $G_m n U_T / I_D$ is plotted versus IC as in Figure 2.

As shown in Figure 4, for short-channel devices subject to VS, the drain current in SI becomes a linear function of the gate voltage, independent of the transistor length. Hence, the transconductance becomes independent of the current and length. Since G_m becomes independent of I_D, and hence of IC, the $G_m n U_T / I_D$ curve scales like $1/(\lambda_c IC)$ in SI (red curve) instead of $1/\sqrt{IC}$ when VS is absent. In essence, the effect of VS is to degrade the transconductance efficiency in SI, meaning that more current is required to obtain the same transconductance than without VS. Nevertheless, irrespective of the channel length, $G_m n U_T / I_D$ remains invariant (i.e. $g_{ms}/IC = 1$) in WI, since short-channel effects (SCEs), including VS, have the same effect on G_m than on I_D simply because G_m is proportional to I_D in WI. As shown in Figure 2, the inversion coefficient for which the SI asymptote of a short-channel device crosses the horizontal unity line is equal to $1/\lambda_c$. As discussed in the next section, this is how the parameter λ_c is extracted from measurements on a short-channel device.

The normalized transconductance efficiency given by (17) is compared to measurements in Figure 8 for the same devices as shown in Figures 4 and 6. Despite that the normalized $G_m n U_T / I_D$ only requires one parameter (λ_c or L_{sat}), the model fits very well to the data over more than five decades of IC.

In a similar way, we can define the G_{ds}/I_D ratio, which from (11) turns out

This article presents the simplified EKV transistor model in saturation since, except for switches, most transistors in CMOS analog circuits are biased in saturation.

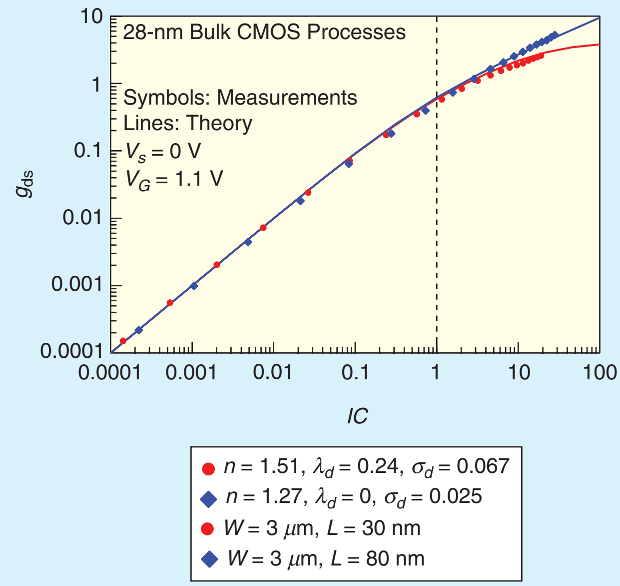

FIGURE 7: Normalized output conductance g_{ds} versus IC measured on minimum and medium length transistors from a 28-nm bulk CMOS process.

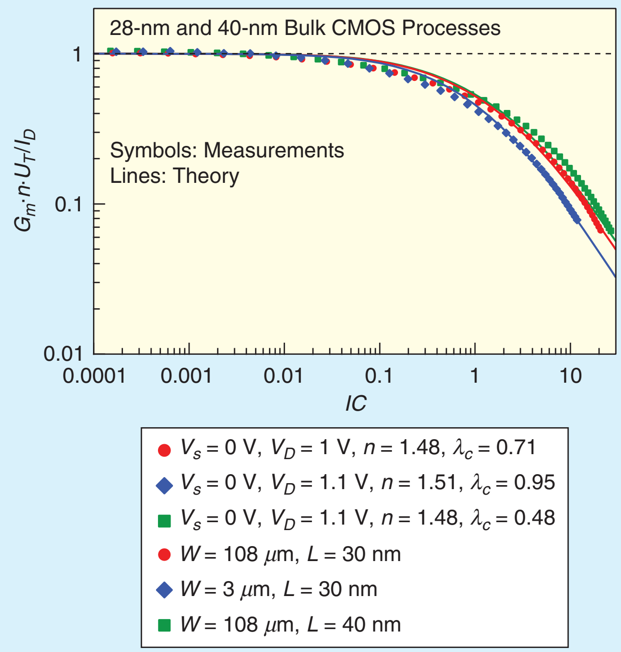

FIGURE 8: Normalized transconductance efficiency g_{ms}/IC versus IC measured on minimum length transistors from a 40-nm and two different 28-nm bulk CMOS processes.

The most important small-signal parameter is without doubt the gate transconductance G_m.

to be about equal to $1/V_M$ for $V_D \ll V_M$. In normalized form, we have

$$\frac{U_T}{V_M} \cong \frac{G_{ds}\,U_T}{I_D} = \frac{g_{ds}}{IC} = \frac{\sigma_d}{n} \cdot \frac{\sqrt{(\lambda_d IC+1)^2+4IC}-1}{IC \cdot [\lambda_d(\lambda_d IC+1)+2]}. \quad (18)$$

From (18), we can deduce that the highest output conductance for a given current is reached in WI and is equal to $G_{ds\text{-}max} \triangleq \sigma_d I_D/(nU_T)$. We can then normalize the output conductance to $G_{ds\text{-}max}$ for the normalized output conductance to reach unity in WI

$$\frac{G_{ds}}{G_{ds\text{-}max}} = \frac{n}{\sigma_d} \cdot \frac{g_{ds}}{IC} = \frac{\sqrt{(\lambda_d IC+1)^2+4IC}-1}{IC \cdot [\lambda_d(\lambda_d IC+1)+2]}. \quad (19)$$

Equation (19) is plotted in Figure 9 and compared to measurements made on the same transistors than in Figure 7 and shows good agreement with the measured data. Note that, unlike for the transconductance, where we want to get the highest transconductance for a given current reached in WI, the output conductance should be minimized for a given current. It will be shown in Part 2 of this article that, even though the output conductance decreases in SI, the self-gain remains actually maximum in WI and simply equal to $1/\sigma_d$.

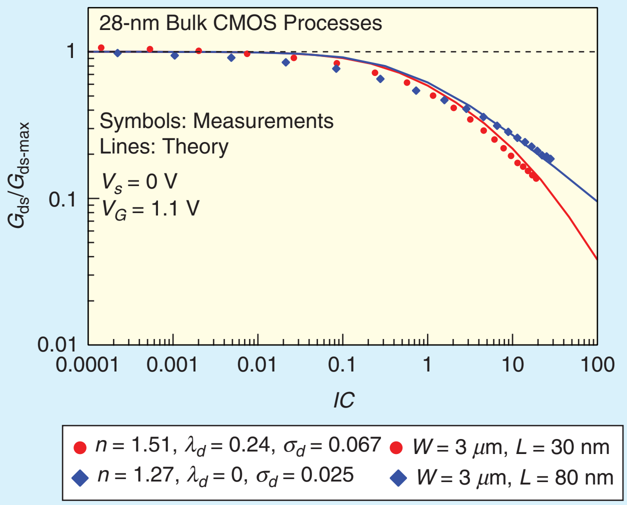

FIGURE 9: Output conductance-to-current ratio $G_{ds}/G_{ds\text{-}max}$ versus IC measured on minimum and medium length transistors from a 28-nm bulk CMOS process.

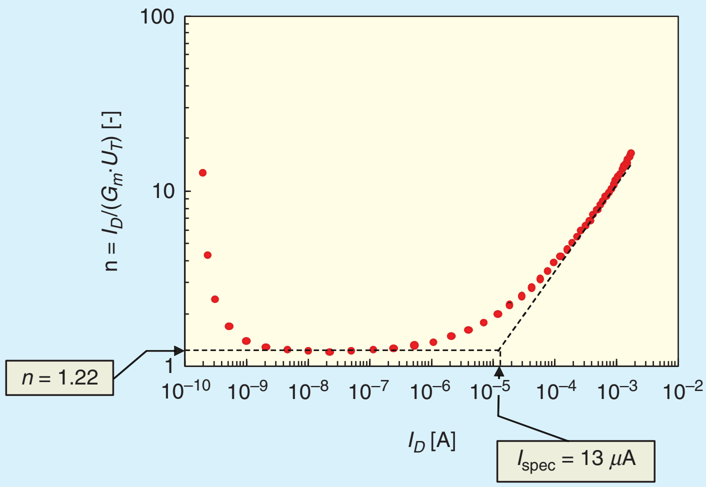

FIGURE 10: The extraction of the slope factor n and the specific current I_{spec}.

Parameter Extraction

The four parameters n, I_{spec}, V_{T0}, and L_{sat} required for fitting the simplified model described in the section "The Large-Signal dc Model" to measured $I_D - V_G$ data can be extracted from measurements following the procedure described below. The extraction starts from the $I_D - V_G$ characteristic measured on a wide and long transistor. After calculating (or measuring) the derivative G_m, the slope factor n is extracted from the plateau reached by the $I_D/(G_m U_T)$ curve in WI as in Figure 10. The specific current for this particular device is then obtained by the intersection between the SI asymptote $\propto \sqrt{I_D}$ and the slope factor horizontal line as shown in Figure 10. For this particular long-channel device, this results in $n = 1.22$ and $I_{spec} = 13\,\mu A$, from which we can derive the specific current per square $I_{spec\square}$ by dividing by the aspect ratio W/L.

The VS parameter λ_c is extracted in Figure 11 from the normalized $G_m n U_T/I_D$ characteristic of a wide and short-channel transistor as the IC corresponding to the intersection of the $1/IC$ asymptote with the unity horizontal line after having properly extracted the slope factor n, which is usually affected by SCEs ($n = 1.48$ in this case compared to $n = 1.22$ as extracted from the long-channel device). This results in $\lambda_c = 0.48$ and hence $L_{sat} = 19.5$ nm for this particular 40-nm transistor.

Finally, the threshold voltage is extracted from the $I_D - V_G$ characteristic to fit the measured data as shown in Figure 4.

The DIBL parameter σ_d used for the output conductance can be extracted in a similar way than the slope factor n by looking at the plateau of the normalized $G_{ds} n U_T / I_D$ curve reached in WI, while the λ_d parameter can be extracted in a similar way than the VS parameter λ_c from the normalized $G_{ds}/G_{ds\text{-max}}$ given by (19) for a short transistor.

Simplified Model Applied to FDSOI and FinFET

Although the simplified model described here was developed for transistors fabricated in a bulk CMOS process, it can also be used for transistors fabricated in an FDSOI process. However, it doesn't model the effect of the additional back gate available in FDSOI processes, and the extracted parameters would be valid only for a single back gate voltage. An example of IC versus $V_G - V_{T0}$ and $G_m n U_T / I_D$ versus IC measured on three different transistor lengths from a 28-nm FDSOI process are shown in Figure 12. Except for some deviation observed on the $G_m n U_T / I_D$ versus IC at high IC values, which is probably due to additional mobility reduction due to vertical field, the match between the model and the measured characteristics is surprisingly good.

The model was even tried with transistors coming from a 28-nm

This article presents the simplified EKV model in saturation and shows that it can successfully model the large- and small-signal behavior over a wide range of bias.

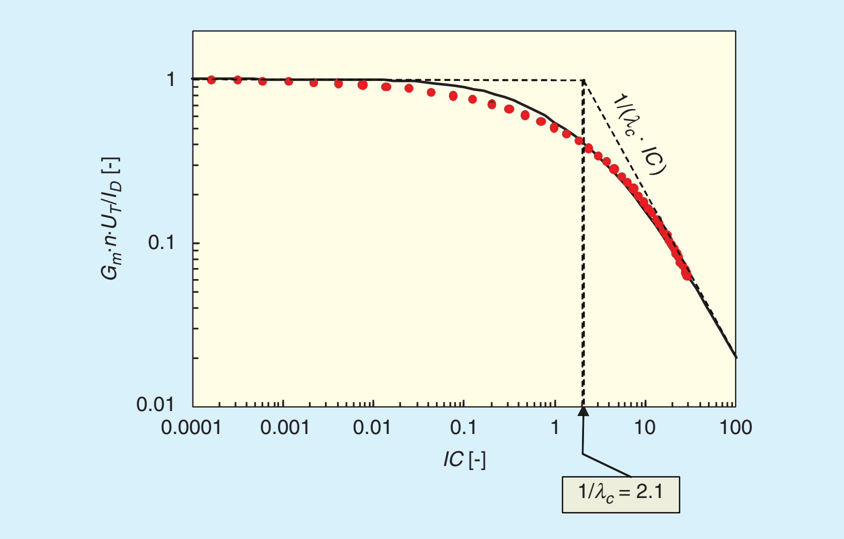

FIGURE 11: The extraction of λ_c on a short device.

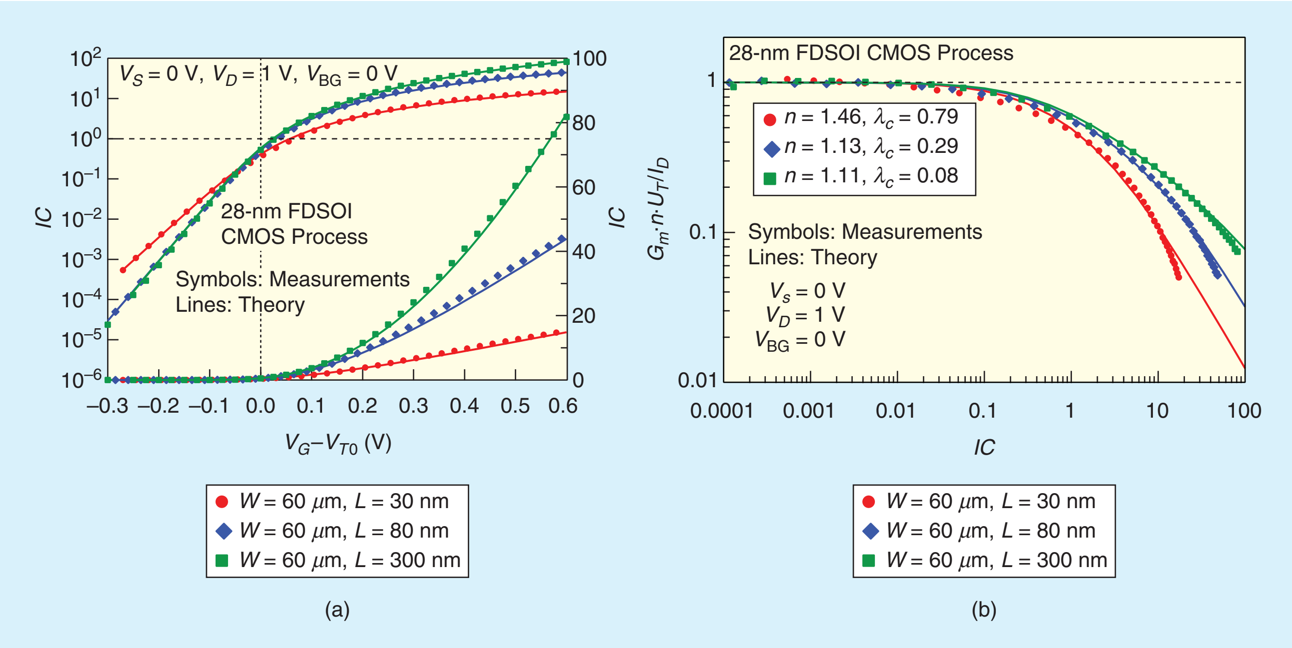

FIGURE 12: The simplified EKV model applied to a 28-nm FDSOI CMOS process. (a) IC versus $V_G - V_{T0}$ and (b) $G_m n U_T / I_D$ versus IC for three different transistor lengths.

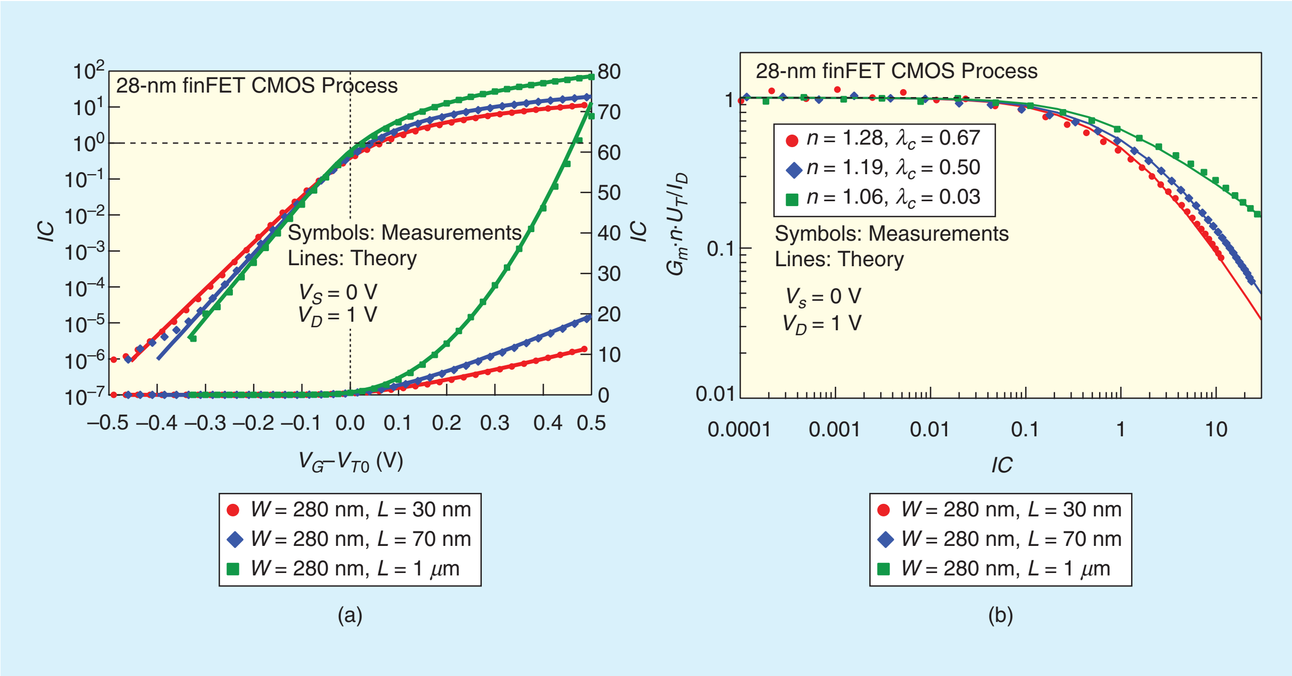

FIGURE 13: The simplified EKV model applied to a 28-nm FinFET CMOS process. (a) IC versus $V_G - V_{T0}$ and (b) $G_m n U_T / I_D$ versus IC for three different transistor lengths.

FinFET process. Figure 13 shows the IC versus $V_G - V_{T0}$ and $G_m n U_T / I_D$ versus IC measured on three different transistor lengths. Again, after proper parameter extraction, the model fits the measured data very well, despite its simplicity.

Conclusions

Analog designers usually like to use simple analytical transistor models to help them identify the optimum bias region in the overall design space where they can pick an initial point close to the optimum target by setting the bias and choosing the transistor size. Further optimization can then be conducted using circuit simulators with the full fetched compact model available in the design kit. Because of the down-scaling of the supply voltage inherent to advanced CMOS technologies, the operating points are pushed more and more toward moderate and even WI, where the standard quadratic model obviously doesn't hold anymore. A simple transistor model valid in all regions of operation from WI to SI is therefore required. This article presents the simplified EKV model in saturation and shows that, despite the very few number of parameters, it can successfully model the large- and small-signal behavior over a wide range of bias.

The concept of inversion coefficient IC is first introduced to replace the overdrive voltage as the main design parameter covering the whole range of operating points from WI to SI across MI. IC is defined as the ratio of the drain current in saturation to the specific current I_{spec}. The latter is proportional to W/L and to the specific current per square $I_{spec\square}$, which is the most important process parameter for the analog designer. It is shown that the specific current can be extracted using a current reference circuit that provides a bias current that allows the inversion coefficient of a given transistor to be precisely set. This bias technique is limited by the transistor matching but is completely independent of the threshold voltage and its variations.

The simplified EKV charge-based model in saturation is then presented, and the $I_D - V_G$ transfer characteristic is validated for different 40- and 28-nm bulk CMOS processes. A very simple expression of the normalized transconductance versus IC is given requiring only a single parameter, the VS parameter λ_c. It is shown that the maximum normalized transconductance reached by a short-channel transistor in SI is simply equal to $1/\lambda_c$. The normalized transconductance efficiency $G_m n U_T / I_D$, which is a key FoM for the design of low-power analog circuit, is then derived as a function of IC. It is shown that the $G_m n U_T / I_D$ characteristic of a short-channel transistor in SI decreases as $1/(\lambda_c IC)$ instead of $1/\sqrt{IC}$ for a long-channel transistor. This means that, because of VS, more current is required to reach the desired transconductance for a short-channel device compared to the ideal case where VS would be absent. Despite that it requires only the VS parameter λ_c, the $G_m n U_T / I_D$ versus IC fits the measured data from 40- and 28-nm bulk CMOS processes extremely well over a large range of bias.

It is then shown that the normalized output conductance $G_{ds} U_T / I_D$

follows the same dependence than the normalized $G_m n U_T / I_D$ characteristic, but with a different parameter λ_d replacing λ_c and an additional parameter σ_d accounting for the effect of DIBL. How to extract all the required parameters from the $I_D - V_G$ and $I_D - V_D$ characteristics measured in saturation on a long- and a short-channel device is presented. Finally, it is concluded that the simplified EKV model can also be used for transistors from a FDSOI and FinFET 28-nm processes.

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