Use the device parameters given in Example 5.3 and the following information for calculating junction capacitances:

$x_{j,N,P} = 0.032\ \mu m$
$\Phi_{0,N,P} = 1.002\ V$
$N_A = 4.8 * 10^{18}\ cm^{-3}$
$N_D = 2.0 * 10^{20}\ cm^{-3}$
$N_A\ (sw) = 10^{17}\ cm^{-3}$

6.8 Consider a CMOS inverter, with the following device parameters:

nMOS	$V_{T0,n} = 0.5\ V$	$\mu_n C_{ox} = 98\ \mu A/V^2$	$E_{C,n}L_n = 0.4\ V$
pMOS	$V_{T0,p} = -0.48\ V$	$\mu_p C_{ox} = 46\ \mu A/V^2$	$E_{C,p}L_p = 1.8\ V$

The power supply voltage is $V_{DD} = 1.2$ V. Both transistors have a channel length of $L_n = L_p = 40$ nm. The total output load capacitance of this circuit is $C_{out} = 200$ fF, which is independent of transistor dimensions.

a. Determine the channel width of the nMOS and the pMOS transistors such that the switching threshold voltage is equal to 0.59 V and the output rise time is $\tau_{rise} = 100$ ps.

b. Calculate the average propagation delay time τ_P for the circuit designed in (a).

c. How do the switching threshold V_{th} and the delay times change if the power supply voltage is dropped from 1.2 to 1.0 V. Provide an interpretation of the results.

6.9 Consider a CMOS inverter with the same process parameters as in Problem 6.8. The switching threshold is designed to be equal to 0.58 V. A simplified expression of the total output load capacitance is given as:

$$C_{out} = 5\ fF + C_{db,n} + C_{db,p}$$

Furthermore, we know that the drain-to-substrate parasitic capacitances of the nMOS and the pMOS transistors are functions of the channel width. A set of simplified capacitance expressions are

$C_{db,n} = 0.16\ fF + 1.7\ W_n$
$C_{db,p} = 0.13\ fF + 1.4\ W_p$

where W_n and W_p are expressed in μm.

a. Determine the channel width of both transistors such that the propagation delay τ_{PHL} is smaller than 35 ps.

b. Assume now that the CMOS inverter has been designed with $(W/L)_n = 10$ and $(W/L)_p = 15$, and that the total output load capacitance is 5 fF. Calculate the output rise time and fall time using the average current method.

6.10 Consider a CMOS inverter with the following parameters:

$V_{T0,n} = 0.5$ V $\quad \mu_n C_{ox} = 98\ \mu$A/V^2 $\quad (W/L)_n = 20$

$V_{T0,p} = -0.48$ V $\quad \mu_p C_{ox} = 46\ \mu$A/V^2 $\quad (W/L)_p = 30$

The power suply voltage is 1.2 V, and the output load capacitance is 10 fF.

a. Calculate the rise time and the fall time of the output signal using the exact method (differential equations) and average current method.

b. Determine the *maximum* frequency of a periodic square-wave input signal so that the output voltage can still exhibit a full logic swing from 0 to 1.2 V in each cycle.

c. Calculate the dynamic power dissipation at this frequency.

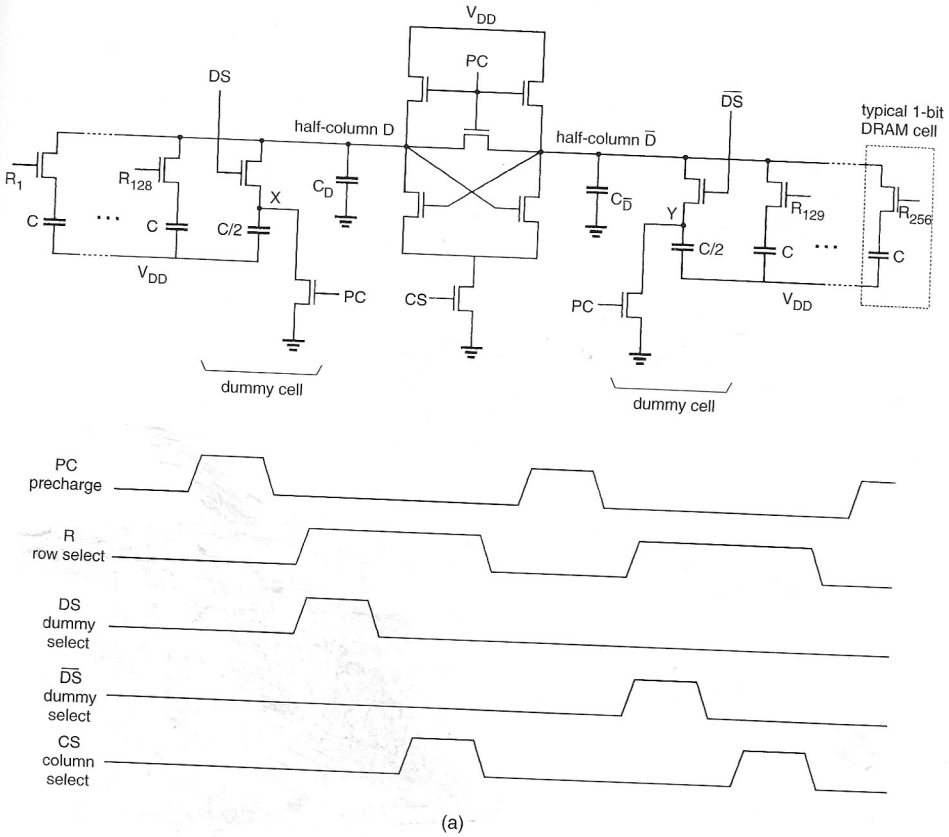
d. Assume that the output load capacitance is mainly dominated by fixed fan-out components (which are independent of W_n and W_p). We want to re-design the inverter so that the propagation delay times are reduced by 25%. Determine the required channel dimensions of the nMOS and the pMOS transistors. How does this re-design influence the switching (inversion) threshold?

the normal and the reference cells, the bit line sense amplifier detects and amplifies the signal difference on bit line pairs to V_{DD} and V_{SS} for full data restoring. The total charge changes to Q_s after the sensing operation and becomes Q_r after the applied field vanishes.

Since the *step-sensing* scheme can cause some reliability issues, a *pulsed-sensing* scheme is also widely used with some read speed penalty, where a pulse is applied instead of keeping the voltage at the plate lines. FRAM suffers from two problems inherent to the ferroelectric material, so-called *fatigue* and *imprint*. The capacitance charge is gradually degraded with the repeated use of the capacitor (*fatigue*) and the ferroelectric capacitor tends to stay at one state preferably over the other when that state is maintained for a long time (*imprint*).

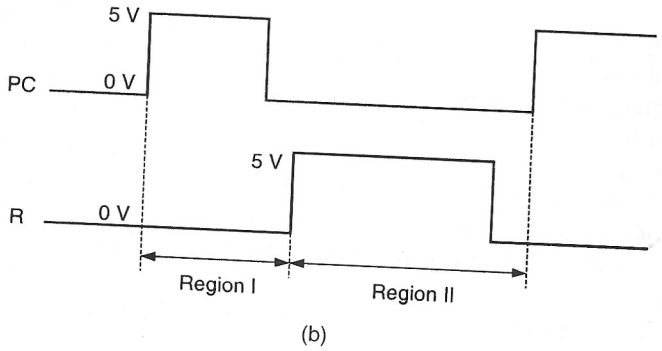
Exercise Problems

10.1 Consider the DRAM circuit shown in Fig. P10.1(a). The threshold voltage of the two precharge transistors is 2 V.



(a)

Figure P10.1a



(b)

Figure P10.1b

Calculate the steady-state voltages of V_D in Regions I and II of Fig. P10.1(b) by assuming the following:

$$C = 50 \text{ fF}$$
$$C_D = 400 \text{ fF}$$
$$V(C) = V(C/2) = V_Y = 0 \text{ V in region I}$$

While PC is high, no other transistor connected to D or $\overline{D}$ is on.

10.2 A single-transistor DRAM cell is represented by the circuit diagram in Fig. P10.2. The bit line can be precharged to $V_{DD}/2$ by using a clocked precharge circuit. Also the WRITE circuit is assumed here to bring the potential of the bit line to V_{DD} or 0 V during the WRITE operation with word line at V_{DD}. Using the parameters given:

$$V_{T0} = 1.0 \text{ V}$$
$$\gamma = 0.3 \text{ V}^{1/2}$$
$$|2\phi_F| = 0.6 \text{ V}$$

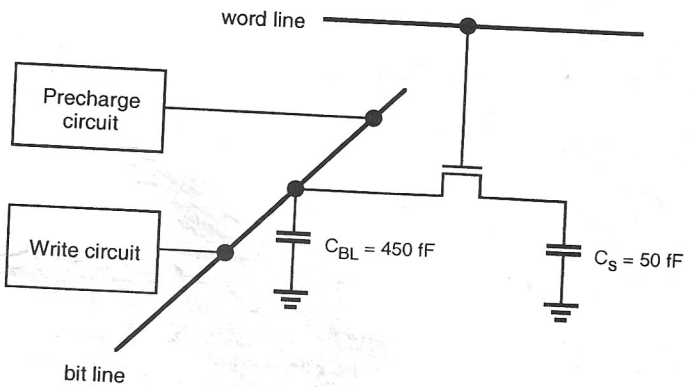


Figure P10.2

a. Find the maximum voltage across the storage capacitor after WRITE-1 operation, i.e., when the bit line is driven to $V_{DD} = 5$ V.

b. Assuming zero leakage current in the circuit, find the voltage at the bit line during READ-1 operation after the bit line is first precharged to $V_{DD}/2$.

10.3 A dynamic CMOS read-only memory (ROM) has been designed with a core array consisting of 64 rows with a pitch of 12 μm and 64 columns with a pitch of 10 μm, as shown in Fig. P10.3. Each column is precharged to 5 V by a pMOS transistor during the interval of zero clock phase and then is pulled down after the clock signal switches to 5 V by one or more nMOS transistors (i.e., NOR implementation) with high gate inputs on the appropriate rows. All of the nMOS transistors have channel widths $W = 4$ μm and source/drain lengths $Y = 5$ μm. As a designer, you are to determine the propagation delay time from a particular input (on row 64) going high to a particular bit line output (on column 64) going low τ_{PHL} between 50% points. Assume that the input signal to row 64 becomes valid-high only after the precharge operation is finished, as shown in the timing diagram. Also, assume that row 64 is running over 30 nMOS transistors and column 64 has 20 nMOS transistors connected to it. For the delay calculation, assume that only one nMOS transistor is pulling down. Also assume that pMOS is strong enough to fully charge the precharging node during the precharge phase of

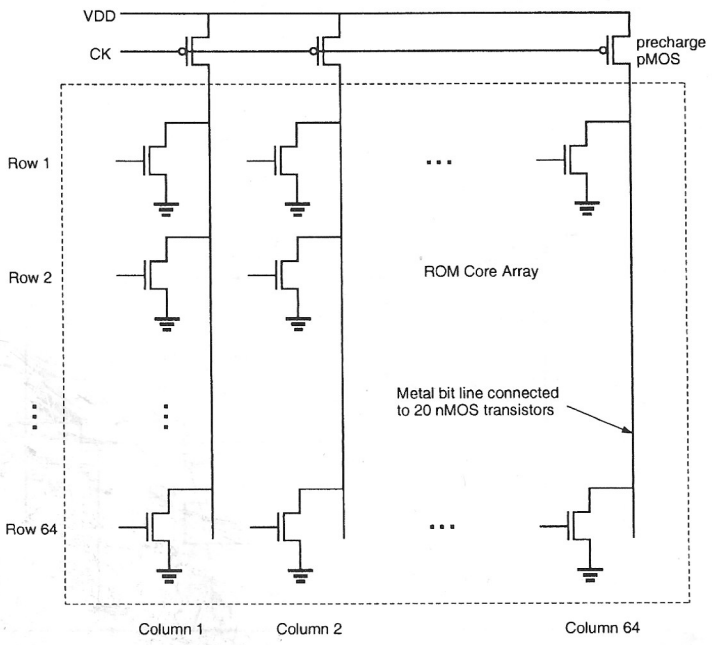


Figure P10.3

the clock signal and to neglect its drain parasitic capacitance. Device parameters are given as

$$C_{jsw} = 250 \text{ pF/m}$$
$$C_{j0} = 80\ \mu\text{F/m}^2$$
$$C_{ox} = 350\ \mu\text{F/m}^2$$
$$L_D = 0.5\ \mu\text{m}$$
$$K_{eq} = 1.0 \text{ for worst-case capacitance}$$
$$C_{metal} = 2.0 \text{ pF/cm and } R_{metal} = 0.03\ \Omega\text{/sq}$$
$$C_{poly} = 2.2 \text{ pF/cm and } R_{poly} = 25\ \Omega\text{/sq}$$
$$\text{Polysilicon line width} = 2\ \mu\text{m}$$
$$\text{Metal line width} = 2\ \mu\text{m}$$
$$k_n' = 20\ \mu\text{A/V}^2$$
$$k_p' = 10\ \mu\text{A/V}^2$$
$$V_{T,n} = -V_{T,p} = 1.0 \text{ V}$$

10.4 Consider the CMOS SRAM cell shown in Fig. P10.4. Transistors M1 and M2 have (W/L) values of 4/4. Transistors M3 and M4 have (W/L) values of 2/4. M5 and M6 are to be sized such that the state of the cell can be changed for $V_C \leq 0.5$ V. Assuming that M5 and M6 are the same size, calculate the required (W/L). Use the following parameters:

$$V_{T0,n} = 0.7 \text{ V}$$
$$V_{T0,p} = -0.7 \text{ V}$$
$$k_n' = 20\ \mu\text{A/V}^2$$
$$k_p' = 10\ \mu\text{A/V}^2$$
$$\gamma = 0.4\ \text{V}^{1/2}$$
$$|2\phi_F| = 0.6 \text{ V}$$

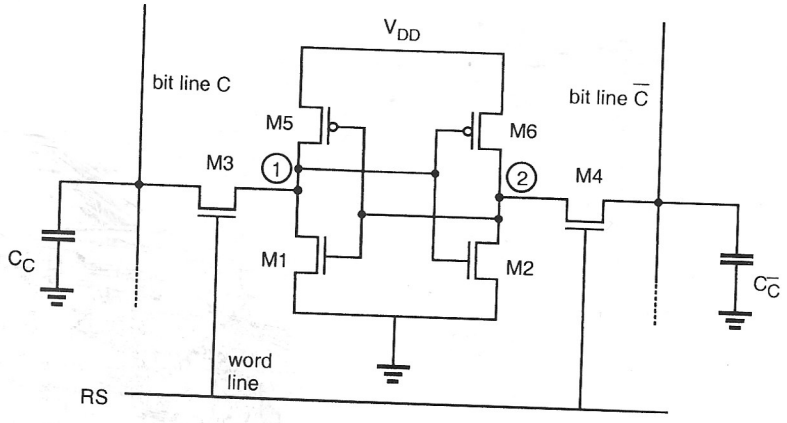


Figure P10.4

10.5 Draw circuit diagrams of the row decoder and the column decoder for an EPROM with four rows and two columns. Use nMOS technology. Develop formulas for the row and column delays in the EPROM. Define any terms in your formulas that are not obvious.

10.6 Consider an 8k × 8k SRAM, which has 64k (= 65536) memory cells and 8 output lines. In the particular SRAM under discussion, 7 address bits go to the row decoder and 6 address bits go to the column decoder. Bit lines are precharged to $V_{DD} = 5$ V before each read operation. A read operation is complete when the bit line has discharged by 0.5 V. A memory cell can provide 1.0 mA of pull-down current to discharge the bit line.

a. Word line resistance is 390 Ω per memory cell. What formula was used to calculate this resistance?

b. Word line capacitance is 22 fF per memory cell. What formula was used to calculate this capacitance?

c. Bit line capacitance is 6 fF per memory cell. What formula was used to calculate this capacitance?

d. Calculate the access time (row delay + column delay) for this SRAM.

e. Describe the operation and design of the word line decoder and the bit line decoder.