Block diagram of a Schmitt trigger circuit. It is a system with positive feedback in which the output signal fed back into the input causes the amplifier A to switch rapidly from one saturated state to the other when the input crosses a threshold.

- A > 1 is the amplifier gain
- B < 1 is the feedback transfer function
\[ V_{th} = V_{T_0} \text{ where } M_0 \text{ turns on, } M_4 \text{ still off} \]
\[ V_L = 1.2 \text{ V} \]
\[ V_{th} = 0.5 \text{ V} \]
\[ V_{in} = 0.4 \text{ V} \]
\[ \frac{V_L}{2} = 0.5 \text{ V} \]
\[ V_{in} \left( V_{T_0} - V_{T_1} \right) + V_{in} \]
\[ = \frac{1}{2} \left( \frac{V_L}{2} \right) \left( V_{T_0} - V_{T_1} \right) + V_{in} \]

It is seen that at this point, M4 is already on. Thus, the previous analysis, which is based on the assumption that M4 is not conducting, can no longer be valid. At this input voltage, node C is being pulled down toward MB. This can also be seen clearly from the simulation results. We conclude that the upper logic threshold voltage \( V_{th} \) is approximately equal to 0.62 V.

Next, we consider negative input voltage, i.e., assume that the input voltage is the.

**Output from Negative Input Voltage**

\[ V_{in} < 0 \text{ V} \]
\[ \text{If } M_0 \text{ and } M_3 \text{ are on, then the output voltage in } V_L = 0 \text{ V. The pull-down transistor M3 and M2 are off, and M0 is in saturation, thus,} \]
\[ E_D = 0 \]
\[ V_L = 0 \text{ V} \]
\[ \text{Solving this equation for } V_L, \text{ we get} \]
\[ V_L = \frac{1}{\beta} \left( V_{in} - 0 \right) \]

The output voltage is still unchanged.

**Output from Negative Input Voltage**

\[ V_{in} > 0 \text{ V} \]
\[ \text{If } M_0 \text{ is on and in saturation region, M3 is also in saturation, thus,} \]
\[ E_D = 0 \]
\[ V_L = 0 \text{ V} \]
\[ \text{Solving this equation for } V_L, \text{ we get} \]
\[ V_L = \frac{1}{\beta} \left( V_{in} - 0 \right) \]

The output voltage is still unchanged.

**Output from Negative Input Voltage**

\[ V_{in} = 0 \text{ V} \]
\[ \text{If } M_0 \text{ is on and in saturation region, M3 is also in saturation, thus,} \]
\[ E_D = 0 \]
\[ V_L = 0 \text{ V} \]
\[ \text{Solving this equation for } V_L, \text{ we get} \]
\[ V_L = \frac{1}{\beta} \left( V_{in} - 0 \right) \]

The output voltage is still unchanged.
Phase locked loop, PLL applications

The phase locked loop take in a signal to which it locks and can then output this signal from its own internal VCO. At first sight this may not appear particularly useful, but with a little ingenuity, it is possible to develop a large number of phase locked loop applications.

Some phase lock loop applications include:

- **FM demodulation**: One major phase locked loop application is that of an FM demodulator. With PLL chips now relatively cheap, this PLL application enables high quality audio to be demodulated from an FM signal.
- **AM demodulation**: Phase locked loops can be used in the synchronous demodulation of amplitude modulated signals. Using this approach, the PLL locks onto the carrier so that a reference within the receiver can be generated. As this corresponds exactly to the frequency of the carrier, it can be mixed with the incoming signal to synchronous demodulate the AM.
- **Indirect frequency synthesizers**: Use within a frequency synthesizer is one of the most important phase locked loop applications. Although direct digital synthesis is also used, indirect frequency synthesis forms one of the major phase locked loop applications.
- **Signal recovery**: The fact that the phase locked loop is able to lock to a signal enables it to provide a clean signal and remember the signal frequency if there is a short interruption. This phase locked loop application is used in a number of areas where signals may be interrupted for short periods of time, for example when using pulsed communications.

The Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and a resulting difference or error voltage is produced. This corresponds to the phase difference between the two signals.

The error signal from the phase detector passes through a low pass filter which governs many of the properties of the loop and removes any high frequency elements on the signal. Once through the filter the error signal is applied to the control terminal of the VCO as its tuning voltage. The sense of any change in this voltage is such that it tries to reduce the phase difference and hence the frequency between the two signals. Initially the loop will be out of lock, and the error voltage will pull the frequency of the VCO towards that of the reference, until it cannot reduce the error any further and the loop is locked.