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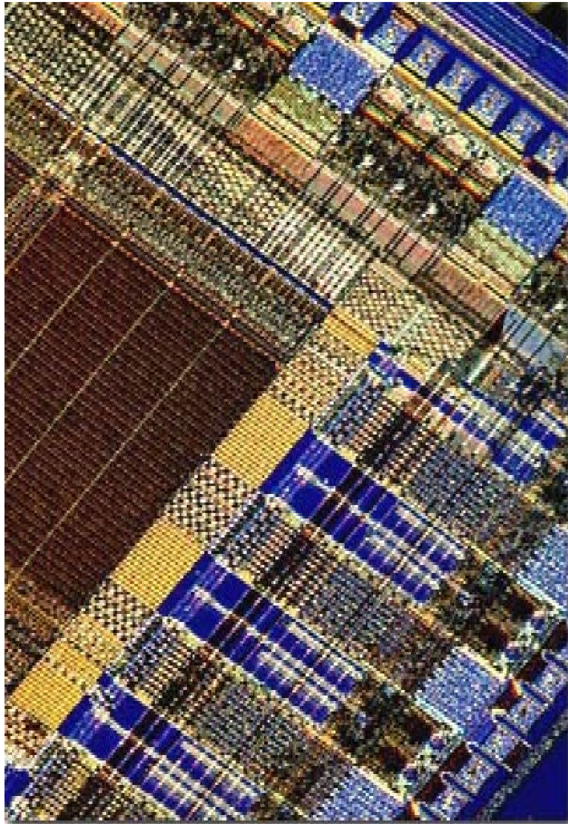

Chapter 10
Semiconductor Memories

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C. Kim

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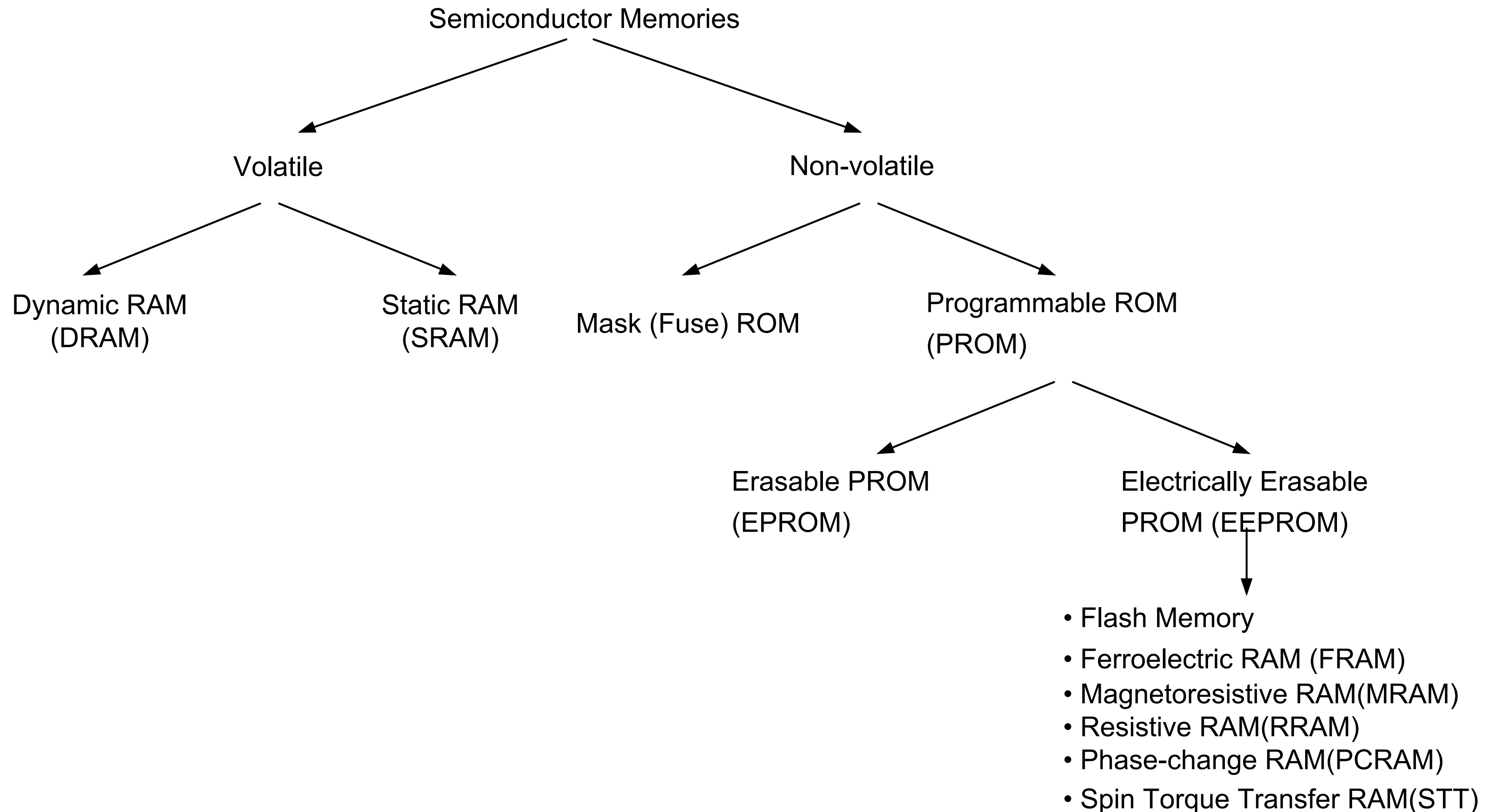
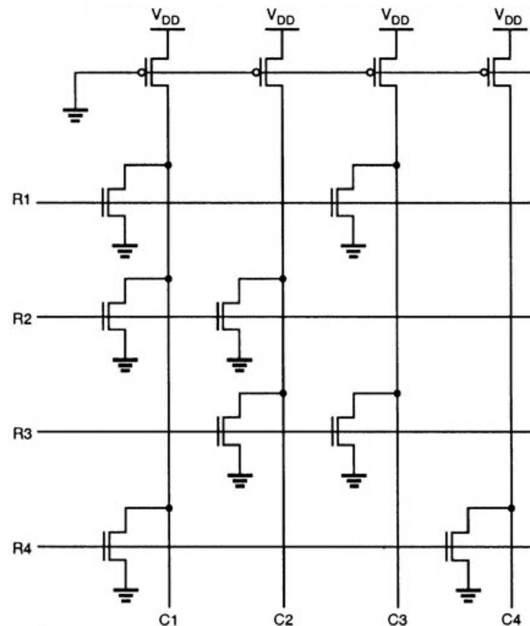
10.1 Introduction

◆ Semiconductor memory types



10.4 Nonvolatile Memory

- Simple combinational Boolean network
- Only one word line selected at a time
- Active transistors exist at cross point
- Dynamic ROM
  - use periodic precharge signal to reduce static power



R1	R2	R3	R4	C1	C2	C3	C4
1	0	0	0	0	1	0	1
0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	1
0	0	0	1	0	1	1	0

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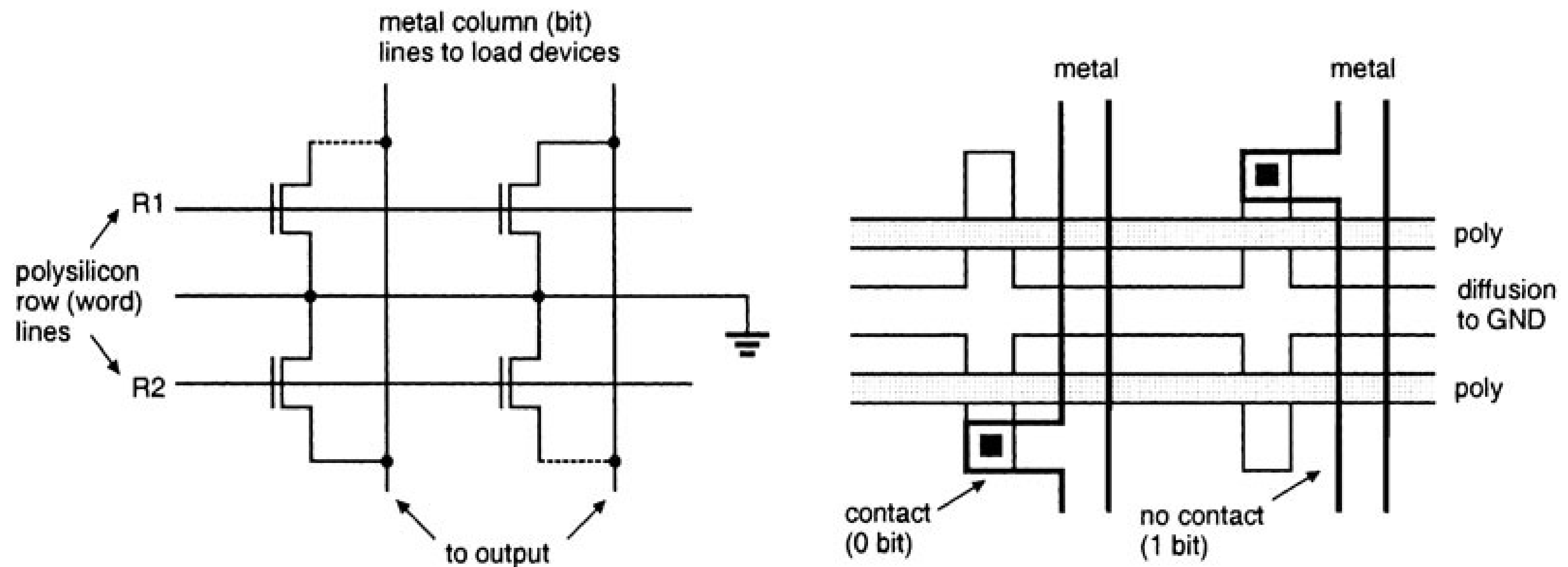
Layout of NOR ROM Array(1)

- Initially, NMOS at every row-column intersection
- '1'-bits are realized by omitting drain or source connection or gate electrode of corresponding NMOS



Layout example of a NOR ROM array

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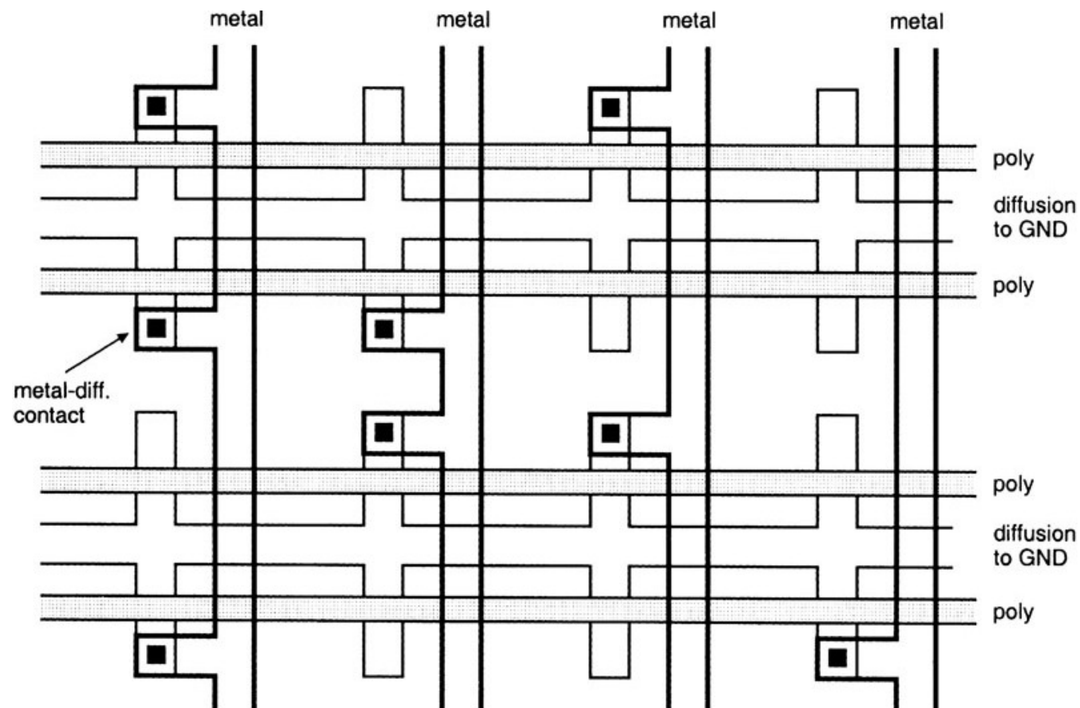
Layout of NOR ROM Array(2)

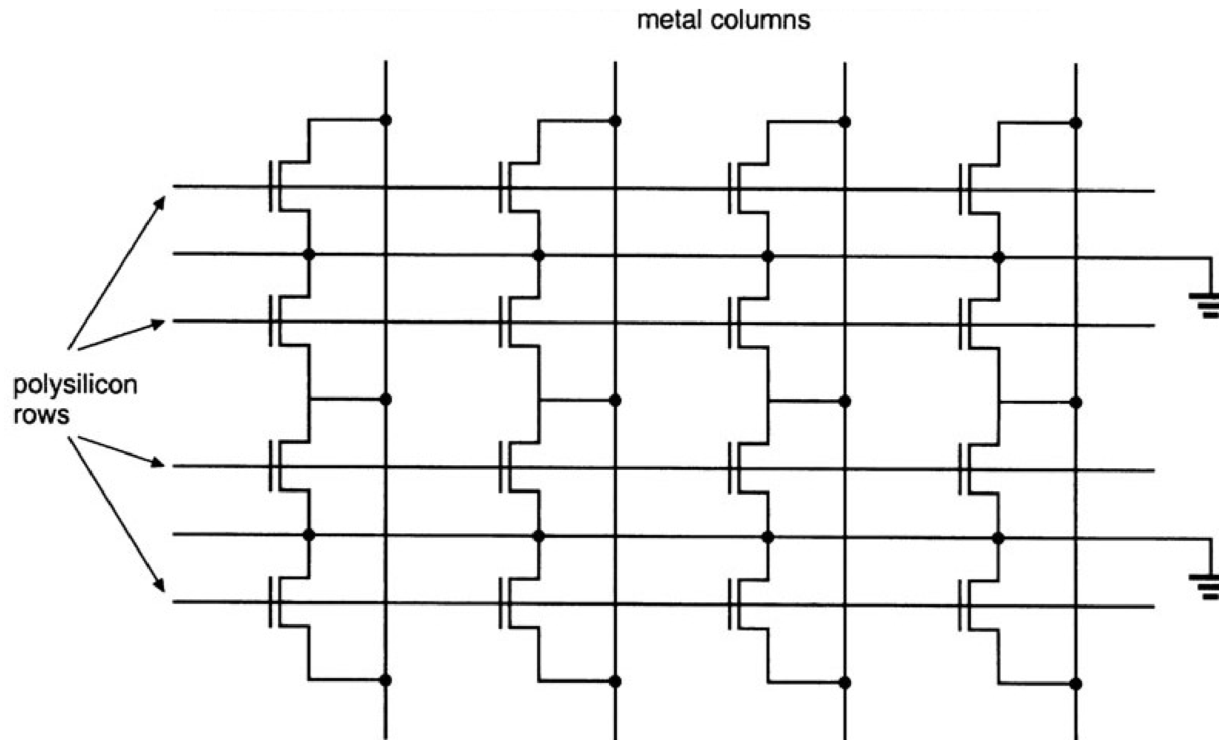
- In reality, metal column lines laid out directly on top of diffusion column to reduce horizontal dimension



Layout of the 4-bit X 4-bit NOR ROM array (pp. 46)

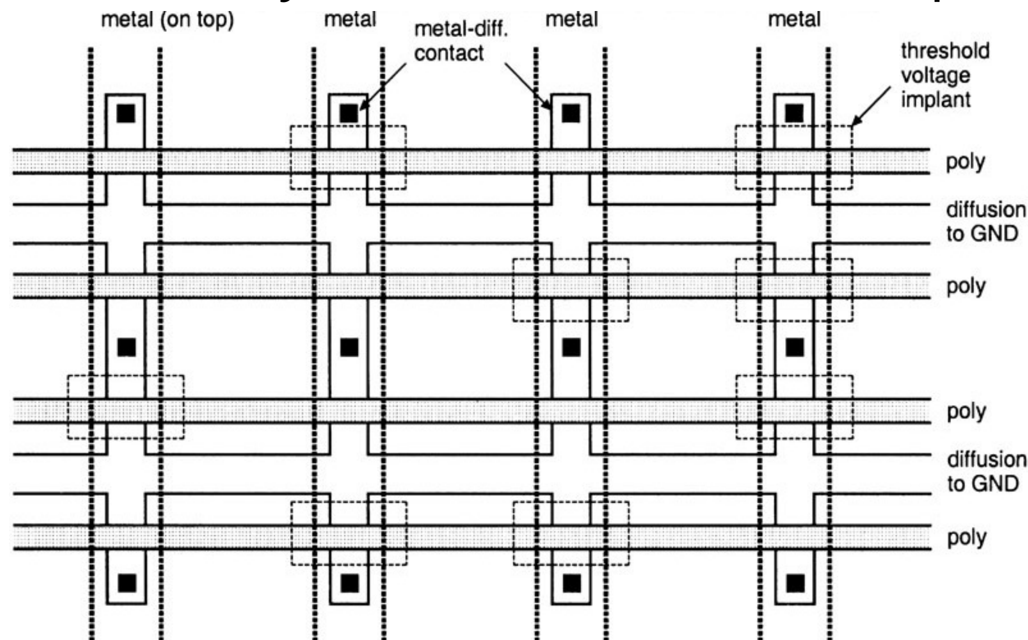
Implant-mask Programmable NOR ROM

- Every two rows share a common ground connection
- Every metal to diffusion contact shared by two adjacent devices



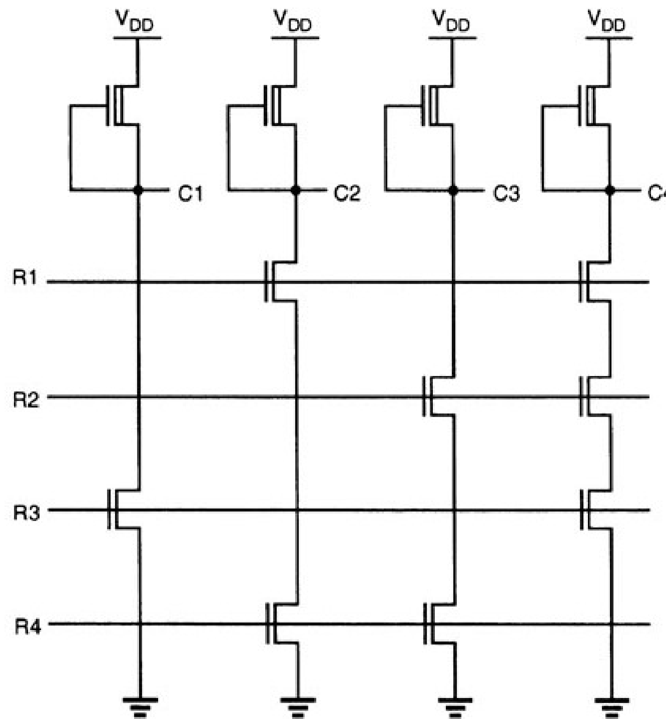
4-bit x 4-bit NOR ROM Array

- Based on implant-mask programming
- Raised threshold voltage >V_{OH} → "1"-bit
- Non-implanted → "0"-bit
- higher core density (smaller silicon area per stored bit)



4-bit x 4-bit NAND ROM Array

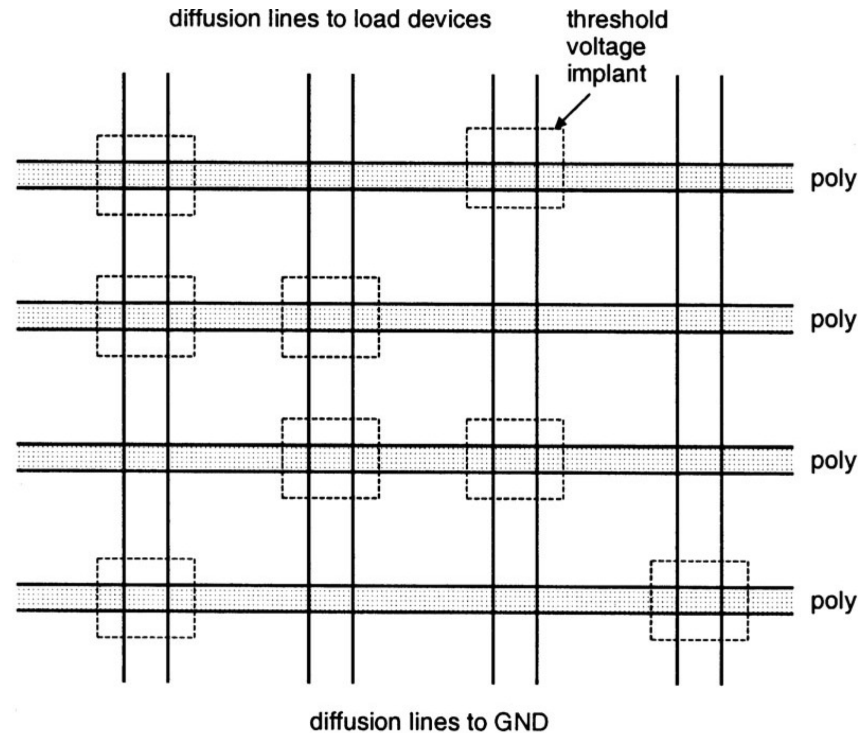
- Bit line : depletion-load NAND gate
- Deactivated transistor → "1"-bit
- Shorted or on transistor → "0"-bit



R1	R2	R3	R4	C1	C2	C3	C4
0	1	1	1	0	1	0	1
1	0	1	1	0	0	1	1
1	1	0	1	1	0	0	1
1	1	1	0	0	1	1	0

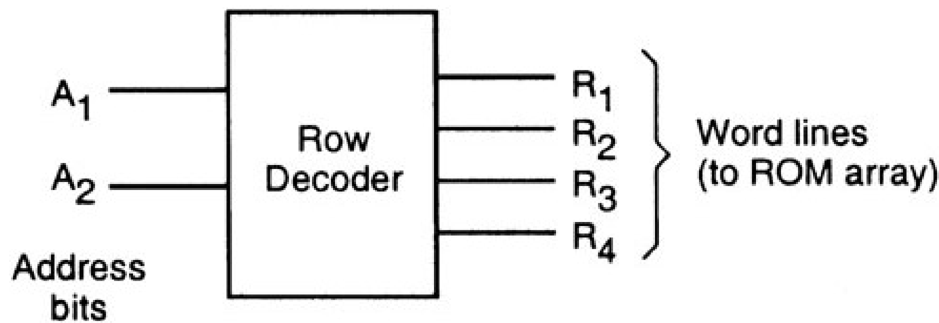
Implant-mask layout of NAND ROM

- Lowered threshold voltage < 0V ➔ "0"-bit
- Much more compact than NOR ROM
- Access time is slower than NOR ROM

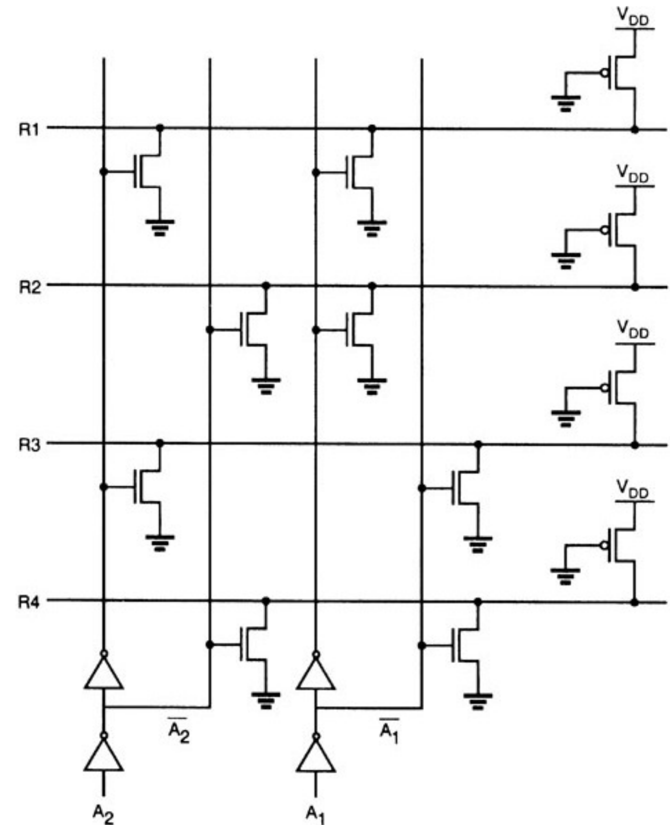


Design of Row and Column Decoders(1)

- Select a particular memory location in array
- Row address decoder example



A_1	A_2	R_1	R_2	R_3	R_4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



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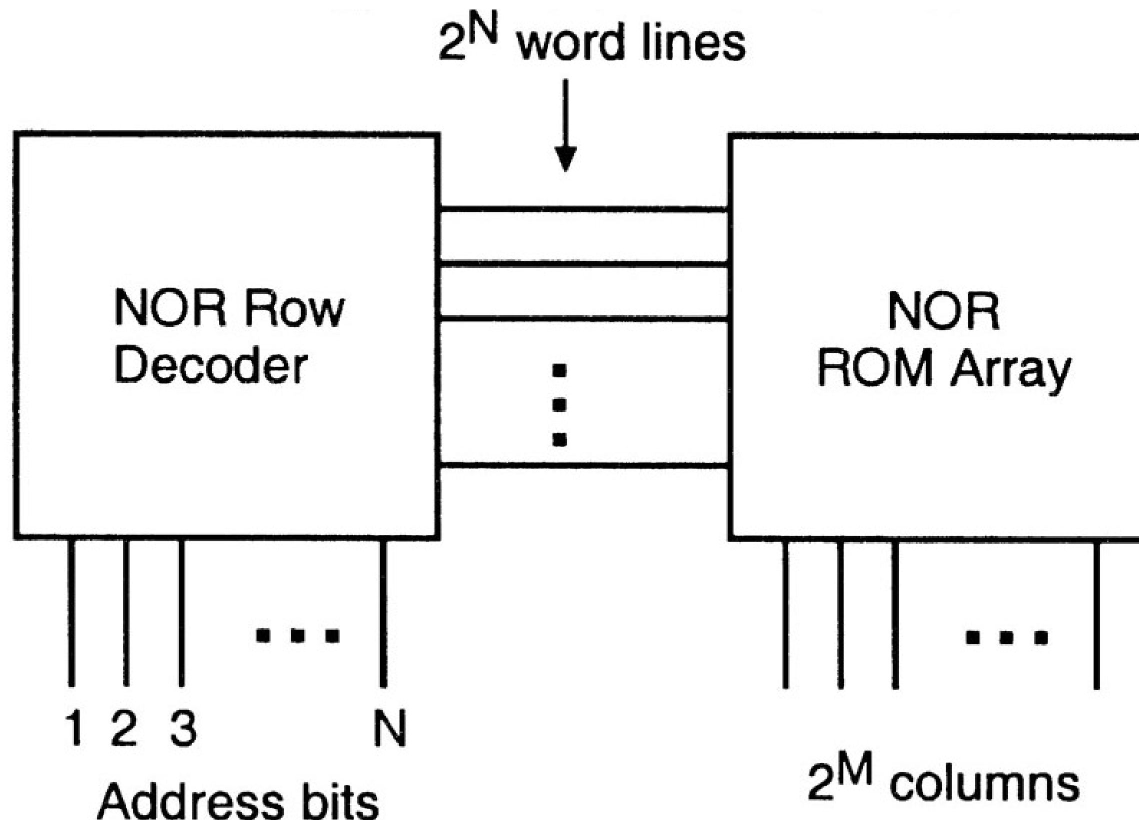
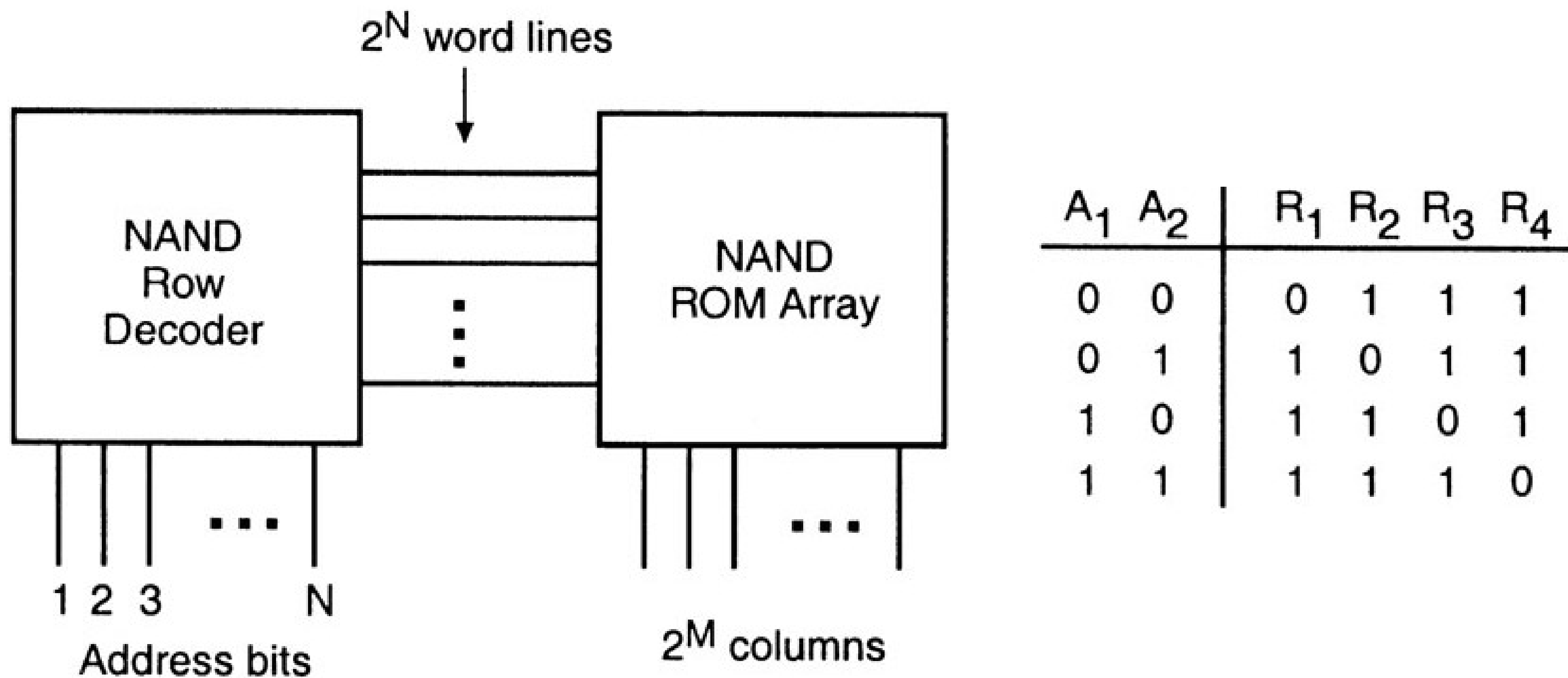
Design of Row and Column Decoders(2)

- ROM array and row decoder (two adjacent NOR arrays)



Row Decoder for NAND ROM

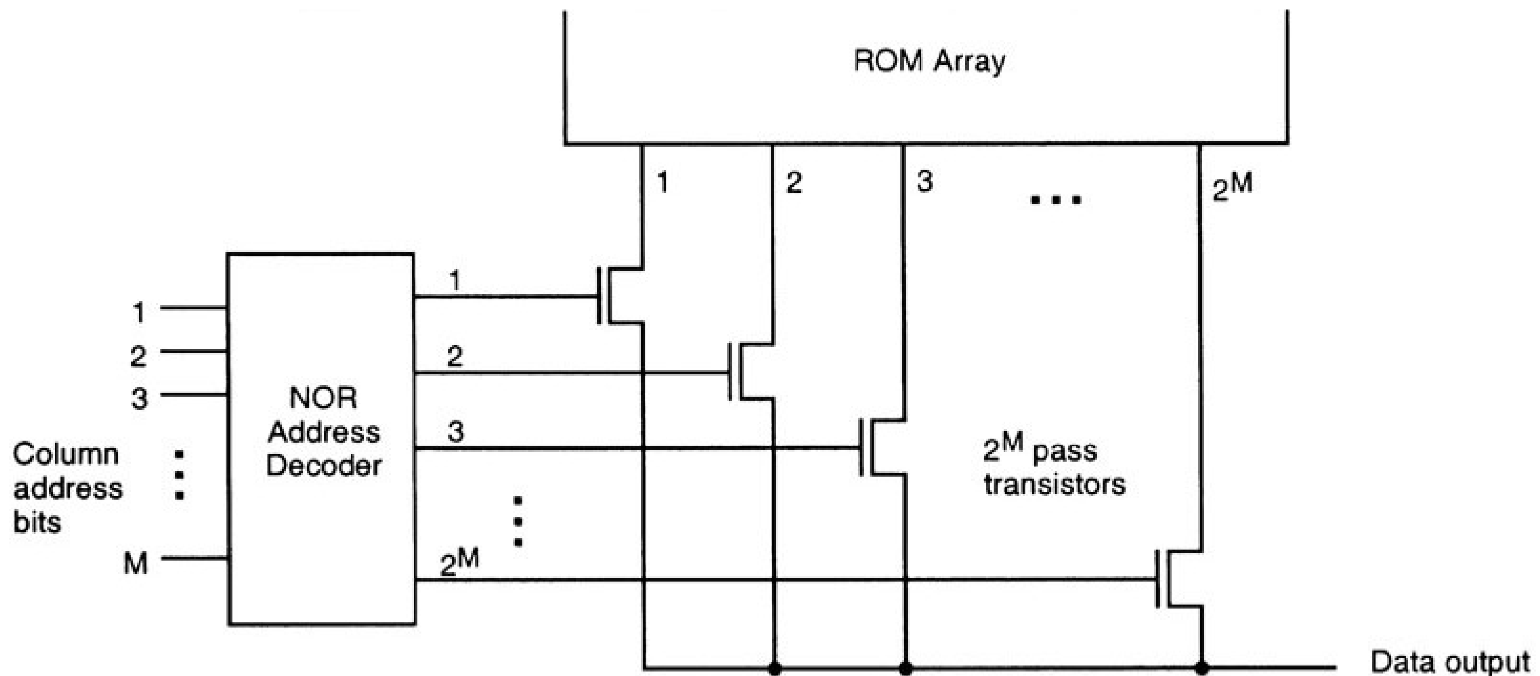
- Lower voltage for logic “0”
- Realized using same layout strategy as memory array



A_1	A_2	R_1	R_2	R_3	R_4
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Column Decoder(1)

- Using NOR address decoder and NMOS pass transistor
- Only one pass transistor turned on at a time
- $2^M(M+1)$ transistors required



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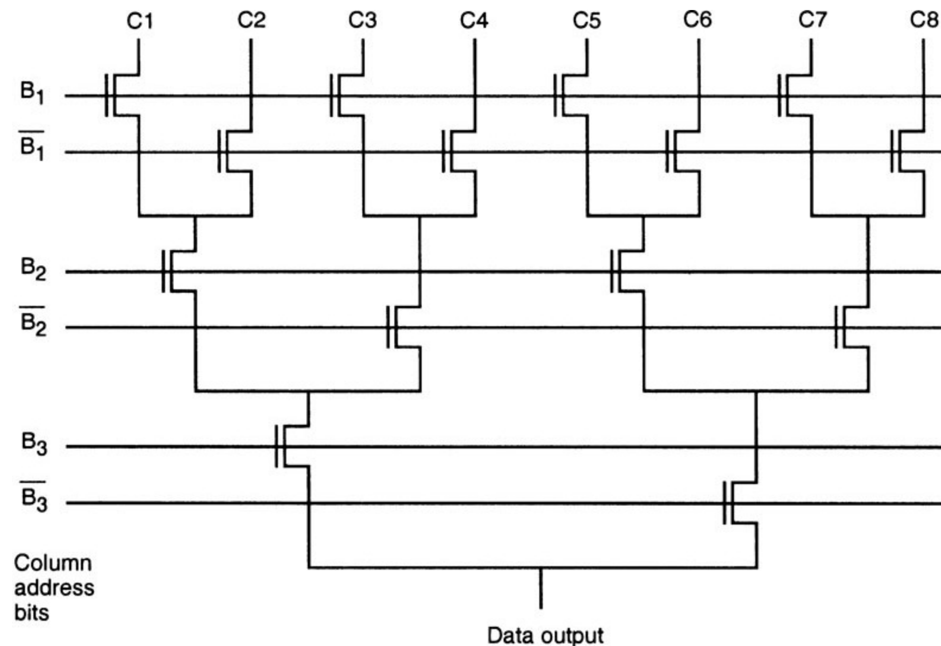
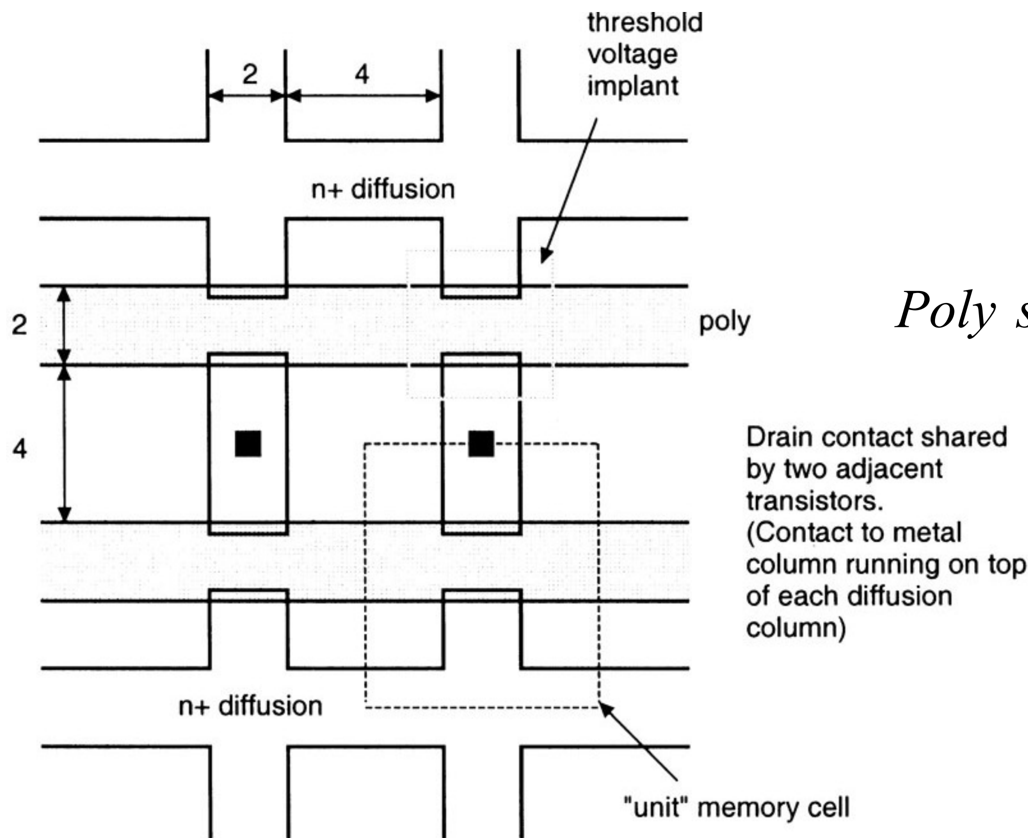
Column Decoder(2)

- Binary selection tree decoder
- NOR address decoder not needed
  - ➔ Reduce the number of transistors significantly
- But, long data access time



Example 10.1(1)

- Analyze the access time of a 32-kbit NOR ROM array



$$\mu_n C_{ox} = 20 \mu A / V^2$$

$$C_{ox} = 3.47 \mu F / cm^2$$

$$Poly\ sheet\ resistance = 20\Omega / square$$

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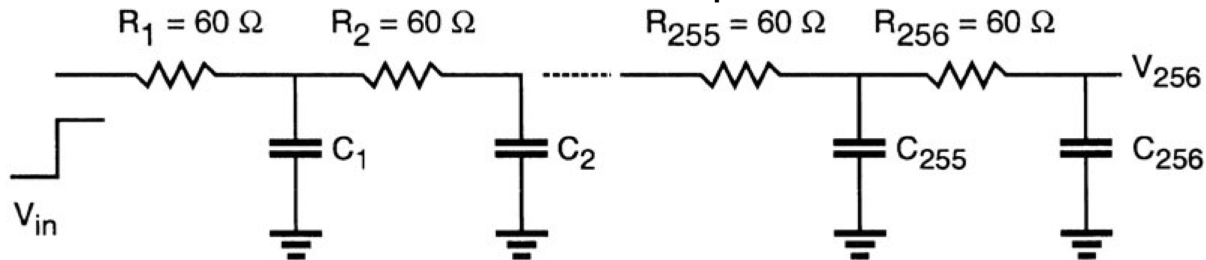
Example 10.1(2)

- Assume 7 row address bits and 8 column address bits (128 rows and 256 columns)
- Calculate row resistance and capacitance



$$C_{row} = C_{ox} \cdot W \cdot L = 10.4\, fF / bit$$

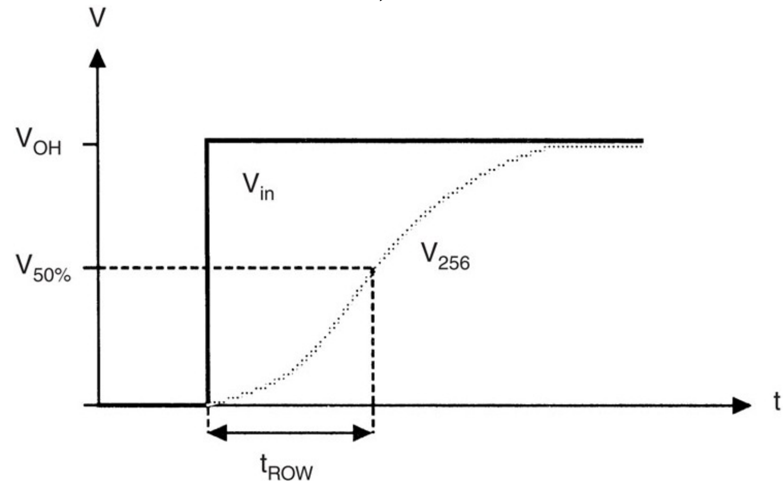
$$R_{row} = (\#\ of\ \ squares) \times (Poly\ \ sheet\ \ resistance) = 60\Omega / bit$$

- Calculate row access time

$$t_{row} \approx 0.38 \cdot R_T \cdot C_T = 15.53ns$$

$$R_T = \sum_{all\ columns} R_i = 15.36k\Omega$$

$$C_T = \sum_{all\ columns} C_i = 2.66\, pF$$



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Example 10.1(3)

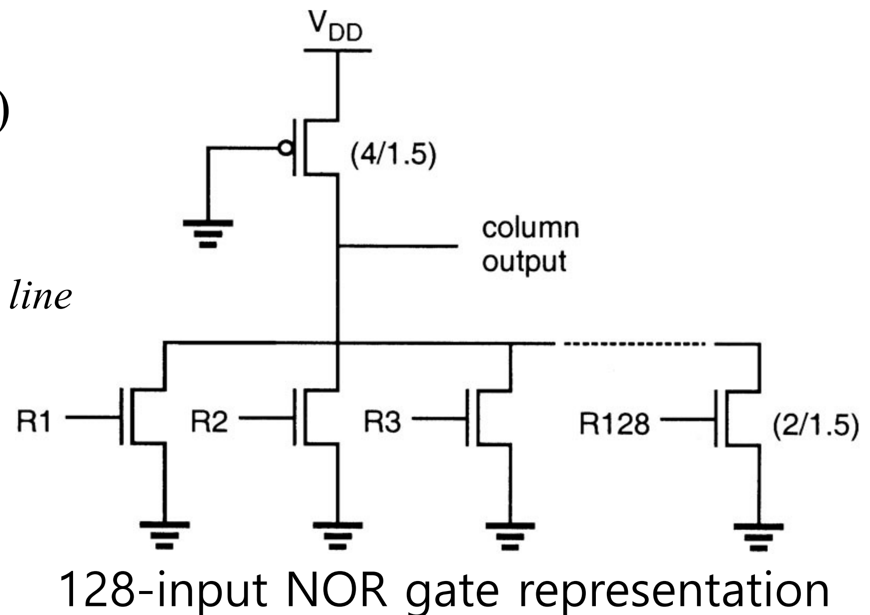
- A more accurate delay: Elmore time constant for RC ladder circuits

$$t_{row} = \sum_{k=1}^{256} R_{jk} C_k = 20.52ns \quad where \quad R_{jk} = \sum_{j=1}^{k} R_j$$

- Calculate column access time

$$C_{column} = 128 \times (C_{gd,driver} + C_{db,driver})$$
$$\approx 1.5pF$$

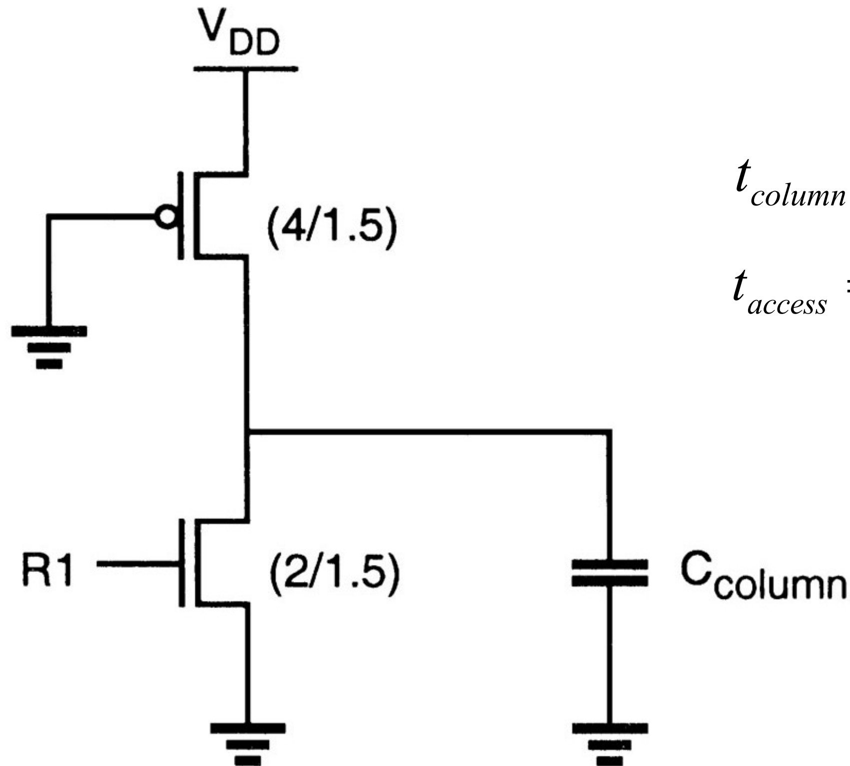
$$where \quad C_{gd,driver} + C_{db,driver} = 0.0118pF / word\ line$$



128-input NOR gate representation

Example 10.1(4)

- To calculate column access time, consider the worst-case signal propagation delay τ_{PHL} for below inverter

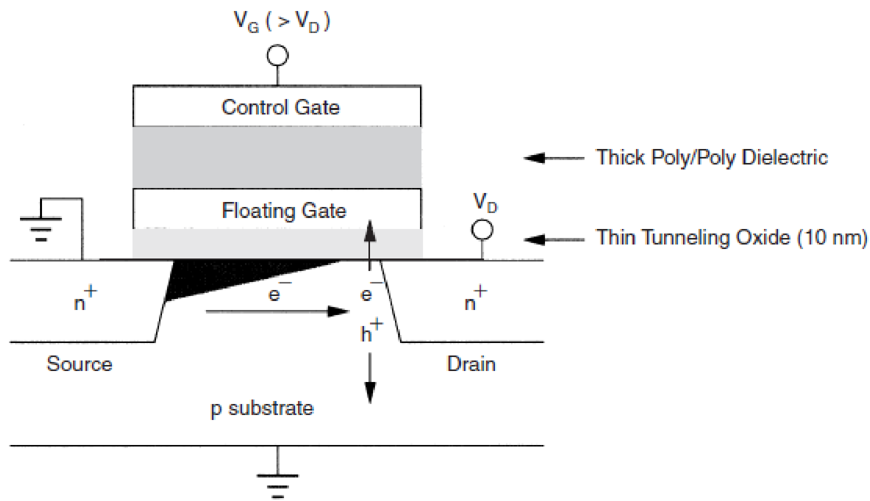


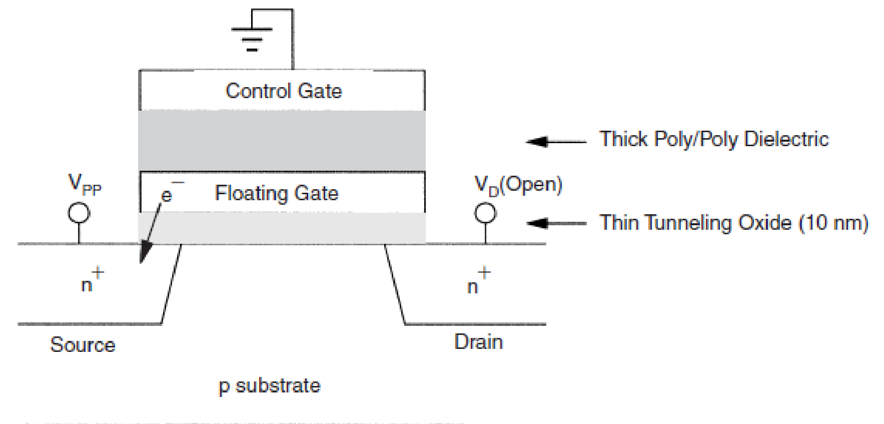
$$t_{column} = 18ns$$ (using eq. 6.18: t_{PHL})

$$t_{access} = t_{row} + t_{column} = 38.5ns$$

10.5 Flash Memory

- One transistor with floating gate
- Memory cell can have two states (two threshold)
- Electron accumulated at the floating gate ➔ higher threshold ➔ "1" state
- Electron removed from the floating gate ➔ lower threshold ➔ "0" state

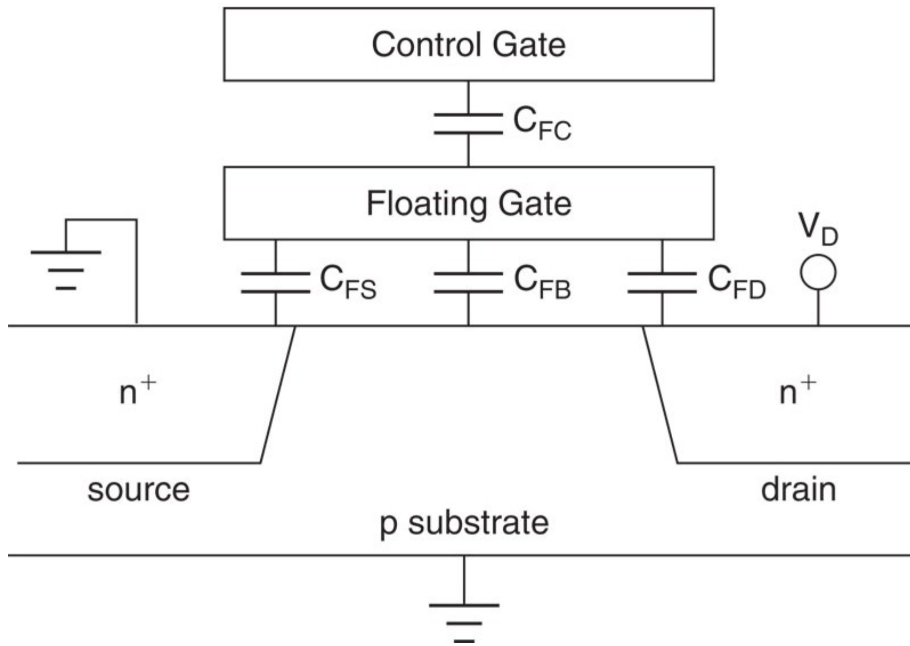




Hot electron injection mechanism (Data programming)

Fowler-Nordheim tunneling mechanism (Data erasing)

Equivalent Capacitive-Coupling Circuit



- V_{FG} by capacitive coupling after V_{CG} & V_D applied

$$V_{FG} = \frac{Q_{FG}}{C_{total}} + \frac{C_{FC}}{C_{total}} V_{CG} + \frac{C_{FD}}{C_{total}} V_D$$

$$C_{total} = C_{FC} + C_{FS} + C_{FB} + C_{FD}$$

- min. V_{CG} to turn on the control gate transistor

$$V_T(CG) = \frac{C_{total}}{C_{FC}} V_T(FG) - \frac{Q_{FG}}{C_{FC}} - \frac{C_{FD}}{C_{FC}} V_D$$

$$\Delta V_T(CG) = -\frac{\Delta Q_{FG}}{C_{FC}}$$

Q_{FC} : charge stored at floating gate
C_{total} : total cap.
C_{FC} : cap. between floating and control gate
C_{FS}, C_{FB} and C_{FD} : cap. between floating gate and source, bulk and drain
V_{CG} and V_D : voltage at control gate and drain
$V_T(FG)$: threshold voltage to turn on the floating gate transistor

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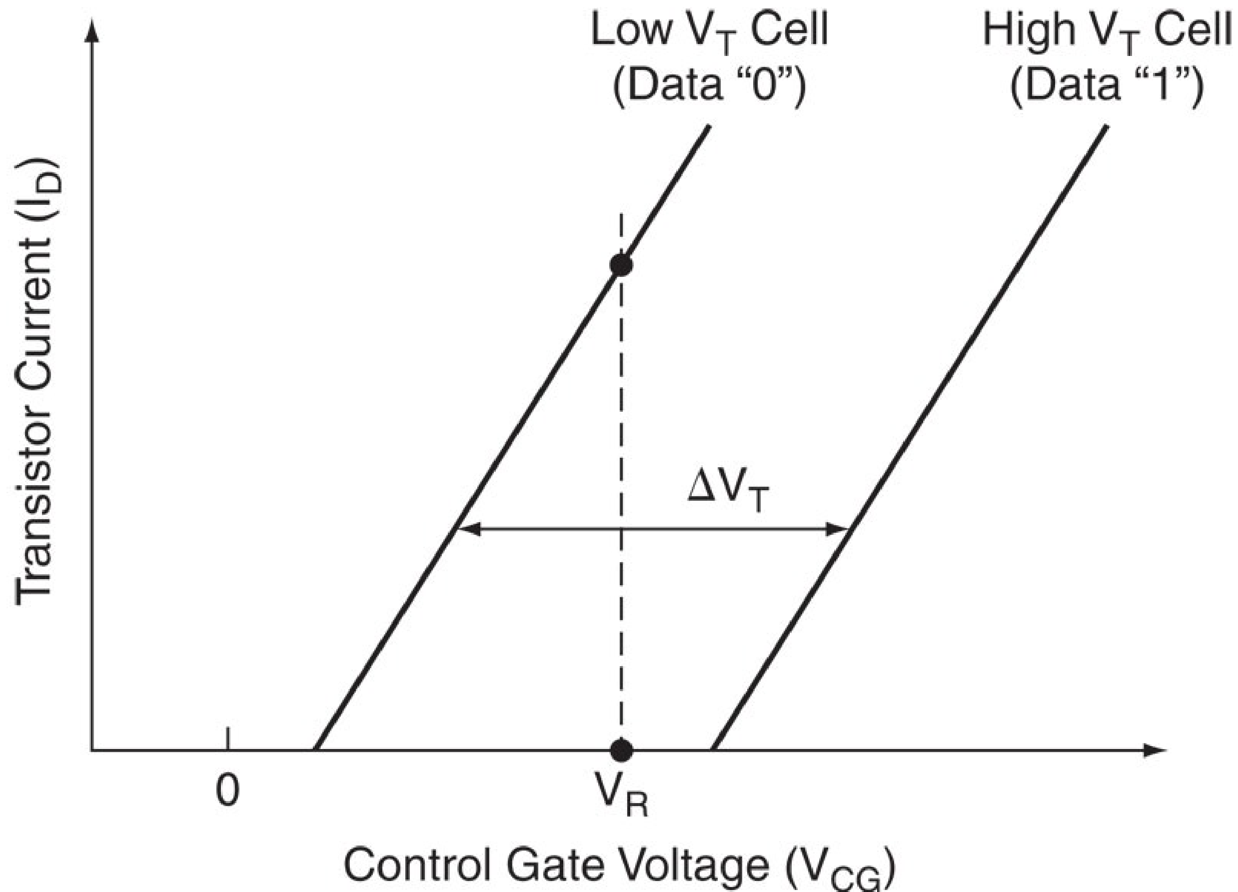
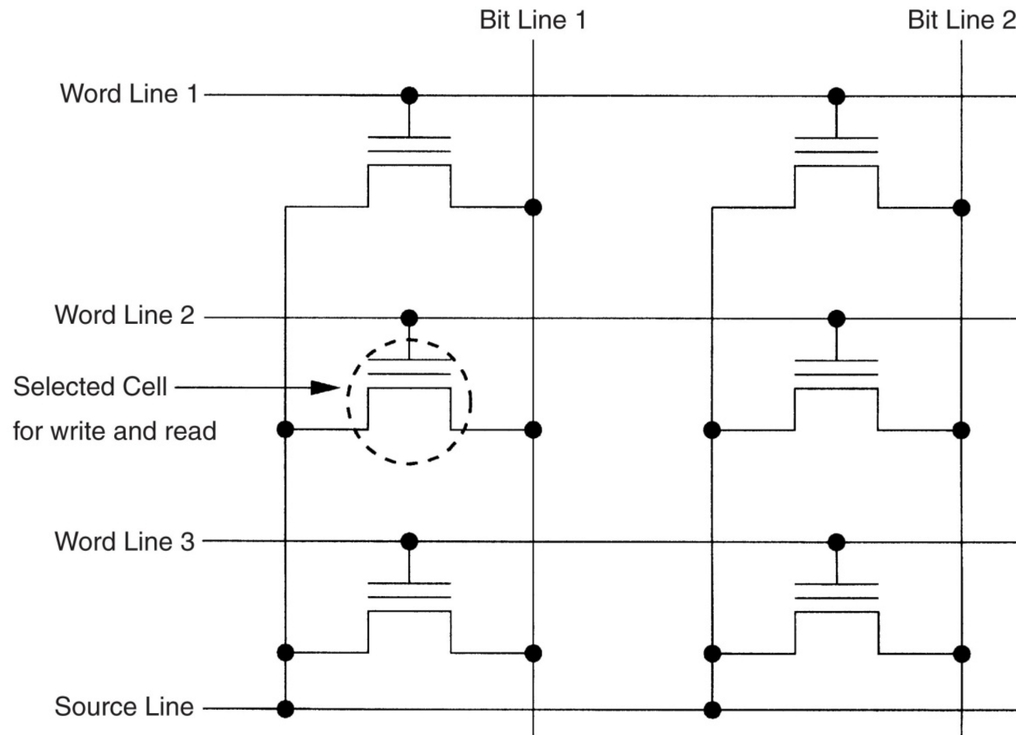
I-V Characteristic of Flash Memory

- Low and high threshold voltages for control gate voltage



NOR Flash Memory Cell

- Bias conditions and configuration of NOR Cells



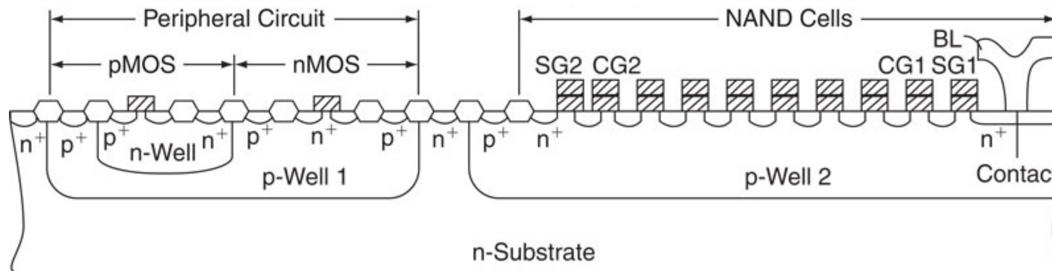
- F-N tunneling mechanism for erase operation
- Hot-electron injection mechanism for programming operation

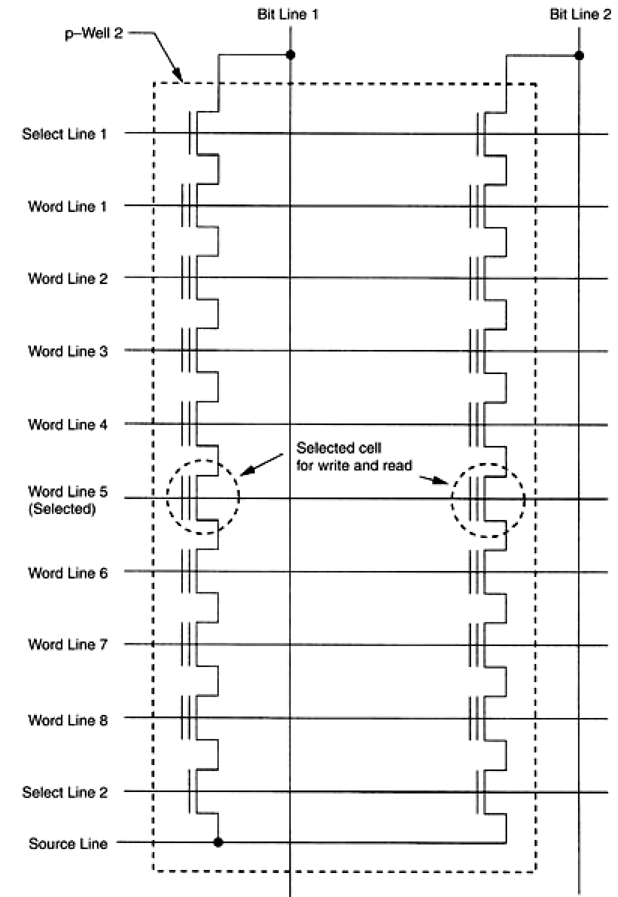
Bias Conditions of NOR Cell

Signal	Operation		
	Erase	Programming	Read
Bit line 1	Open	6V	1V
Bit line 2	Open	0V	0V
Source line	12V	0V	0V
Word line 1	0V	0V	0V
Word line 2	0V	12V	5V
Word line 3	0V	0V	0V

NAND Flash Memory Cell

- Cross-section view and configuration of NAND cells





- F-N tunneling mechanism for erase
- F-N tunneling mechanism for program
- Slower programming and read speed but smaller area than NOR cell structure

Bias Conditions of NAND Cell

Signal	Operation		
	Erase	Programming	Read
Bit line 1	Open	0V	1V
Bit line 2	Open	0V	1V
Select line 1	Open	5V	5V
Word line 1	0V	10V	5V
Word line 2	0V	10V	5V
Word line 3	0V	10V	5V
Word line 4	0V	10V	5V
Word line 5	0V	20V	0V
Word line 6	0V	10V	5V
Word line 7	0V	10V	5V
Word line 8	0V	10V	5V
Select line 2	Open	0V	5V
Source line	Open	0V	0V
p-well 2	20V	0V	0V
n-sub	20V	0V	0V

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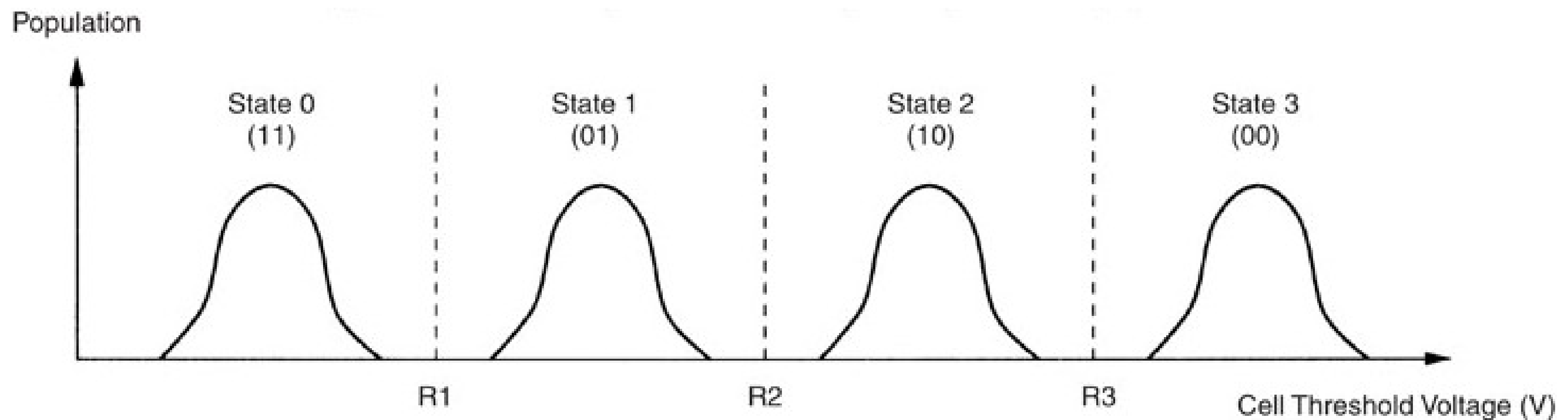
Comparison between NOR and NAND

	NOR	NAND
Erase method	F-N tunneling	F-N tunneling
Programming method	Hot electron injection	F-N tunneling
Erase speed	Slow	Fast
Program speed	Fast	Slow
Read speed	Fast	Slow
Cell size	Large	Small
Scalability	Difficult	Easy
Application	Embedded system	Mass storage

Multilevel Cell Concept

- Effective memory density can be improved
- Possible state number limited by
  - Available charge range
  - Accuracy of programming and read operations
  - Disturbance of state over time

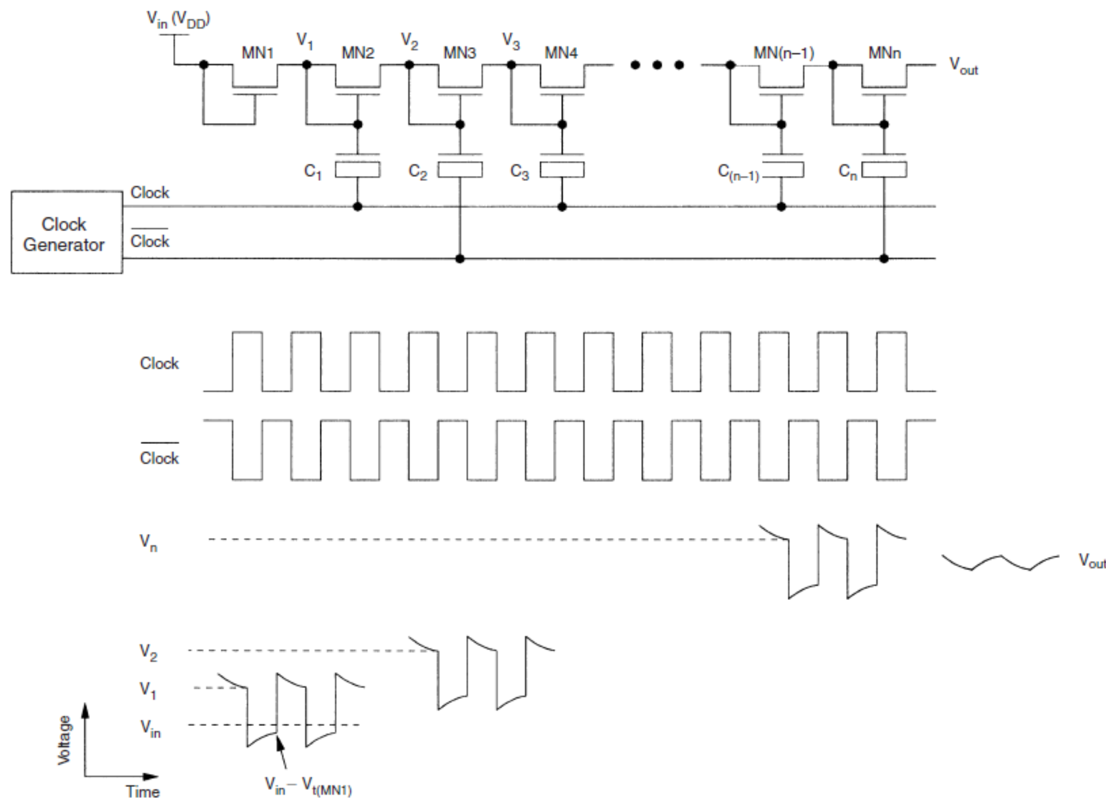


Threshold voltage distribution of 2bits/cell storage

Flash Memory Circuit

- On-chip charge pump used to generate programming voltage
- Chain of diode and cap. to charge or discharge each half cycle

$$V_{out} = V_{in} + (\gamma V_{DD} - V_T(MN1)) + \cdots + (\gamma V_{DD} - V_T(MNn))$$



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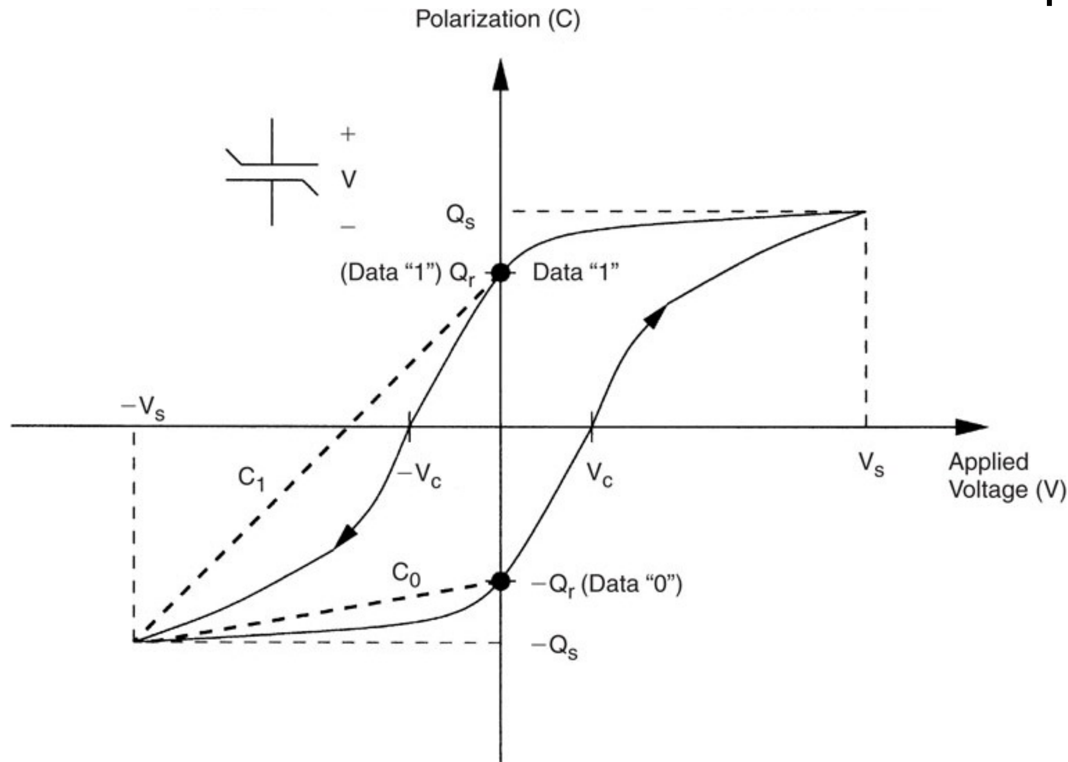
10.6 Ferroelectric Random Access Memory

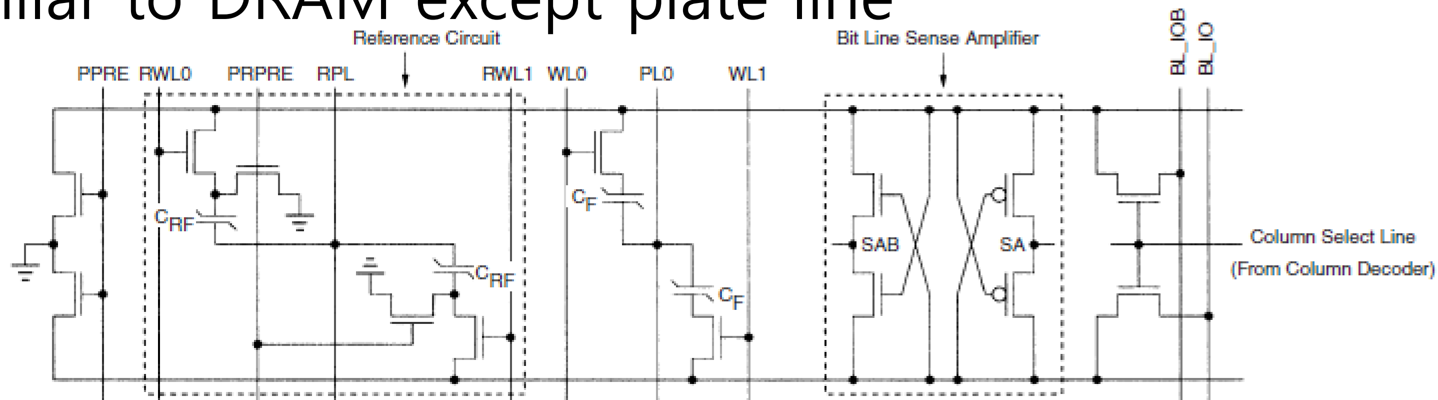
- Hysteresis characteristic of a ferroelectric cap.

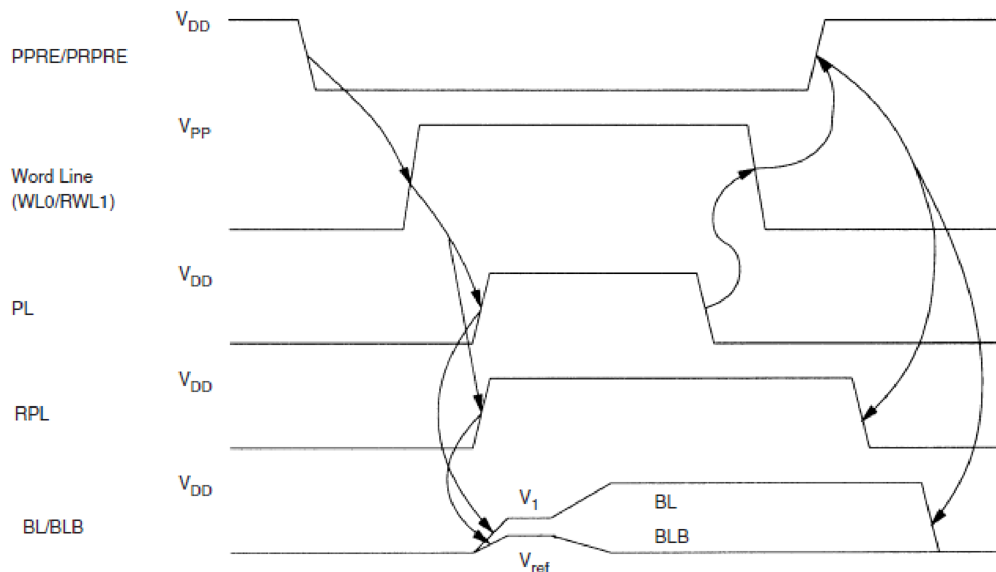


- Total charge varies as function of applied voltage

Structure and Operation of FRAM

- Similar to DRAM except plate line





- Step-sensing scheme

$$\Delta V_1 = \frac{C_1}{C_1 + C_{BL}} V_{DD}$$

$$\Delta V_0 = \frac{C_0}{C_0 + C_{BL}} V_{DD}$$

C_1 and C_0 : linearly modeled ferroelectric cap

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Problems of FRAM

- Step-sensing scheme cause reliability issues
  - Pulse sensing scheme also used with read speed penalty
- Fatigue
  - Capacitance charge gradually degraded with repeated use
- Imprint
  - Ferroelectric cap tends to stay at one state preferably when state maintained for a long time