The CAD category of design rules checking includes the tools for layout rules checking, electrical rules checking, and reliability rules checking. The layout rules checking program has been highly effective in weeding out potential yield problems and circuit malfunctions.

Exercise Problems

1.1 An ADD/SUBTRACT logic circuit is shown in Fig. P1.1. It performs the ADD operation for P = 0 and SUBTRACT for P = 1.

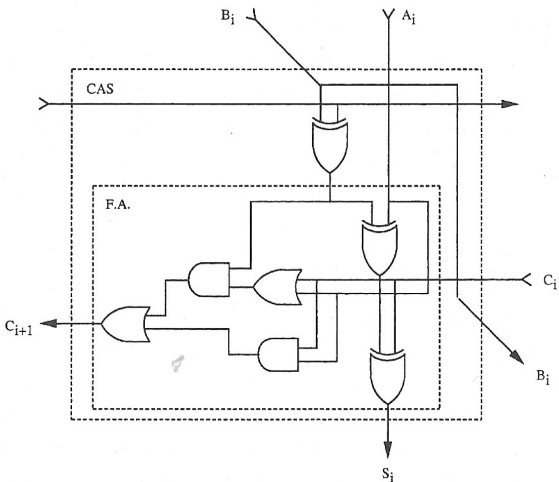

Figure P1.1

a. Draw an equivalent CMOS logic diagram by noting that most CMOS gates, except for the transmission gate and XOR, are inverting. For example, the AND gate is implemented with NAND followed by an inverter.

b. By using the gate array platform given in Fig. 1.30, implement the CMOS circuit as compactly as possible with the aspect ratio, which is the ratio of vertical dimension to horizontal dimension, as close to 1 as possible.

1.2 For the CMOS circuit in Problem 1.1,

a. First develop a small library of CMOS cells.

b. Place the cells into a single row and interconnect them with proper ordering such that the total interconnection wire length is minimized.

1.3 A measure of design productivity predicts the required engineer-months in terms of design implementation styles, such as repeated transistors (RPT), non-repeatable unique transistors (UNQ), PLA, RAM, and ROM transistors; the experience level of engineers (yr); the productivity improvement per year (D);

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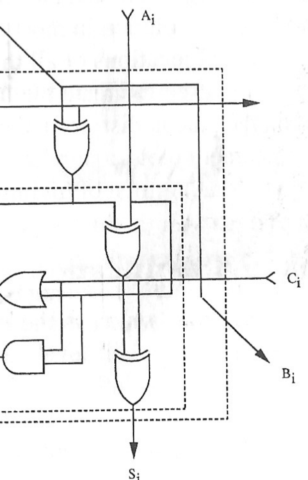

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and the design complexity (H). The formula proposed by Fey is

$$Engineer - Months(EM) = (1 + D)^{-yr}[A + Bk^H]$$

where the number k of equivalent transistors in the design is expressed by

$$k = UNQ + C \cdot RPT + E \cdot PLA + F\sqrt{RAM} + G\sqrt{ROM}$$

In this formula, the transistor count is in units of thousands and the coefficients A, B, C, D, E, F, G, and H are model parameters that depend on the designers' experience and CAD tool support. The parameter (*yr*) represents the number of years since the extraction time of the model parameters. A set of sample values for these parameters are A = 0, B = 12, C = 0.13, D = 0.02, E = 0.37, F = 0.65, G = 0.08, and H = 1.13.

a. Discuss how one would extract the model parameters within a design organization.

b. A 24-bit floating-point processor has been designed using 20,500 repeated transistors, 10,500 unique transistors, 105,500 RAM transistors, and 150,200 ROM transistors. Calculate the expected engineer-months (*EM*) by assuming the experience year value of $yr = 3$. Note that the transistor counts in the formula are in units of thousands, for instance, UNQ = 10.5, not 10,500.

1.4 A large-scale, fast prototyping system has been produced by using a very large array of field programmable logic arrays (FPGAs).

a. Discuss the pros (features) and cons (weaknesses) of such prototyping systems for proof of design concepts and verification in view of effort and speed performance of the design.

b. How would you compare the hardware prototyping method with the computer simulation method?

1.5 As the design complexity increases with increasing number of on-chip transistors, the on-chip noises have become more pronounced. Discuss the impact of packaging in suppressing on-chip noises in view of the numbers and strategic placement of ground and power pads, and the numbers of ground and power planes.

1.6 The testing of VLSI chips at speed has become increasingly more difficult due to undesirable parasitic effects in a testing environment. Also the cost of high-speed testing machines has become very high and, hence, in reality it is difficult for smaller manufacturers to procure such equipment. Discuss what problem the chip testing only at lower speed would cause for systems houses that take such chips to develop systems at speed. What alternative ways can be used to ease the problem in the absence of at-speed testers?

To take the given drain voltage variation into account, we must now calculate the voltage equivalence factors, K_{eq} and $K_{eq}(sw)$, for both types of junctions, which allows us to find the average large-signal capacitance values.

$$K_{eq} = -\frac{2\sqrt{1.11}}{-1-(-0.1)}\cdot\left(\sqrt{1.11+1}-\sqrt{1.11+0.1}\right) = 0.675$$

$$K_{eq}(sw) = -\frac{2\sqrt{1.19}}{-1-(-0.1)}\cdot\left(\sqrt{1.19+1}-\sqrt{1.19+0.1}\right) = 0.682 \cong K_{eq}$$

The total area of the n^+/p junctions is calculated as the sum of the bottom area and the sidewall area facing the channel region.

$$A = (0.3\times 0.15)\mu m^2 + (0.15\times 0.032)\mu m^2 = 0.05\mu m^2$$

The total length of the n^+/p^+ junction perimeter, on the other hand, is equal to the sum of three sides of the drain diffusion area. Thus, the combined equivalent (average) drain-substrate junction capacitance can be found as

$$\langle C_{db}\rangle = A\cdot C_{j0}\cdot K_{eq} + P\cdot C_{jsw}\cdot K_{eq}(sw)$$

$$= 0.05\times 10^{-8}cm^2\cdot 54.1\times 10^{-8}F/cm^2\cdot 0.675$$

$$+ 0.75\times 10^{-4}cm\cdot 6.38\times 10^{-12}F/cm\cdot 0.682 = 0.509\times 10^{-15}F = 0.509fF$$

Exercise Problems

3.1 Consider a MOS system with the following parameters:

$t_{ox} = 1.6$ nm

$\phi_{GC} = -1.04$ V

$N_A = 2.8\cdot 10^{18}$ cm^{-3}

$Q_{ox} = q4.10^{10}$ C/cm^2

a. Determine the threshold voltage V_{T0} under zero bias at room temperature ($T = 300$ K). Note that $\varepsilon_{ox} = 3.97\varepsilon_0$ and $\varepsilon_{si} = 11.7\varepsilon_0$.

b. Determine the type (p-type or n-type) and amount of channel implant (N_I/cm^2) required to change the threshold voltage to 0.6 V.

3.2 Consider a diffusion area that has the dimensions 0.4 μm $\times$ 0.2 μm and the abrupt junction depth is 32 nm. Its n-type impurity doping level is $N_D = 2.10^{20}$ cm^{-3} and the surrounding p-type substrate doping level is $N_A = 2.10^{20}$ cm^{-3}. Determine the capacitance when the diffusion area is biased at 1.2 V and substrate is biased at 0 V. In this problem, assume that there is no channel-stop implant.

3.3 Describe the relationship between the mask channel length, L_M, and the electrical channel length, L. Are they identical? If not, how would you express L in terms of L_M and other parameters?

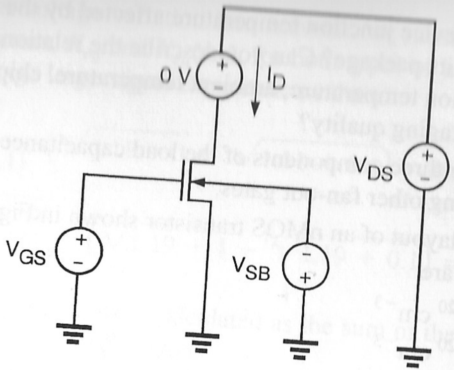

Figure P3.7

3.8 Compare the two technology scaling methods, namely (1) the constant electric field scaling and (2) the constant power supply voltage scaling. In particular, show analytically by using equations how the delay time, power dissipation, and power density are affected in terms of the scaling factor, S. To be more specific, what would happen if the design rules change from, say, 1 μm to $1/S$ μm ($S > 1$)?

3.9 A pMOS transistor was fabricated on an n-type substrate with a bulk doping density of $N_D = 2 \times 10^{16}$ cm^{-3}, gate doping density (n-type poly) of $N_D = 10^{20}$ cm^{-3}, $Q_{ox}/q = 4.10^{10}$ cm^{-2}, and gate oxide thickness of $t_{ox} = 1.6$ nm. Calculate the threshold voltage at room temperature for $V_{SB} = 0$. Use $\varepsilon_{si} = 11.7\varepsilon_0$.

3.10 Using the parameters given, calculate the current through two nMOS transistors in series (see Fig. P3.10), when the drain of the top transistor is tied to V_{DD}, the source of the bottom transistor is tied to $V_{SS} = 0$, and their gates are tied to V_{DD}. The substrate is also tied to $V_{SS} = 0$ V. Assume that $W/L = 10$ for both transistors and $L = 4$ μm.

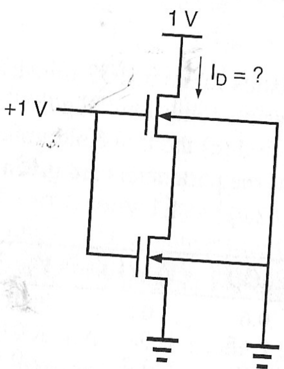

Figure P3.10

3.4 How is the device junction temperature affected by the power dissipation of the chip and its package? Can you describe the relationship between the device junction temperature, ambient temperature, chip power dissipation, and the packaging quality?

3.5 Describe the three components of the load capacitance C_{load}, where a logic gate is driving other fan-out gates.

3.6 Consider a layout of an nMOS transistor shown in Fig. P3.6. The process parameters are

$N_D = 2.10^{20}$ cm^{-3}
$N_A = 2.10^{20}$ cm^{-3}
$X_j = 32$ nm
$L_D = 10$ nm
$t_{ox} = 1.6$ nm
$V_{T0} = 0.53$ V

Channel stop doping = 16.0 × (*p*-type substrate doping)

Find the effective drain parasitic capacitance when the drain node voltage changes from 1.2 to 0.6 V.

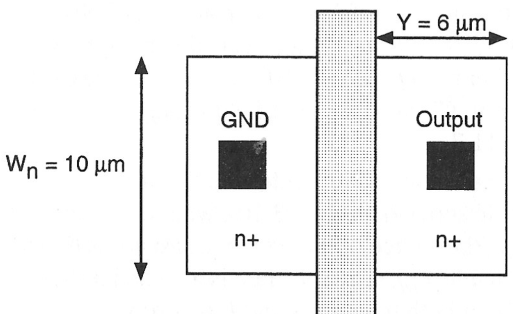

Figure P3.6

3.7 A set of *I–V* characteristics for an nMOS transistor at room temperature is shown for different biasing conditions. Figure P3.7 shows the measurement setup. Using the data, find (a) the threshold voltage V_{T0} and (b) velocity saturation v_{sat}. Some of the parameters are given as $W = 0.6$ μm, $E_cL = 0.4$ V, $\lambda = 0.05$, $t_{ox} = 16$ Å, $|2\phi_F| = 1.1$ V.

V_{GS} (V)	V_{DS} (V)	V_{SB} (V)	I_D (μA)
0.6	0.6	0.0	6
0.65	0.6	0.0	12
0.9	1.2	0.3	44
1.2	1.2	0.3	156