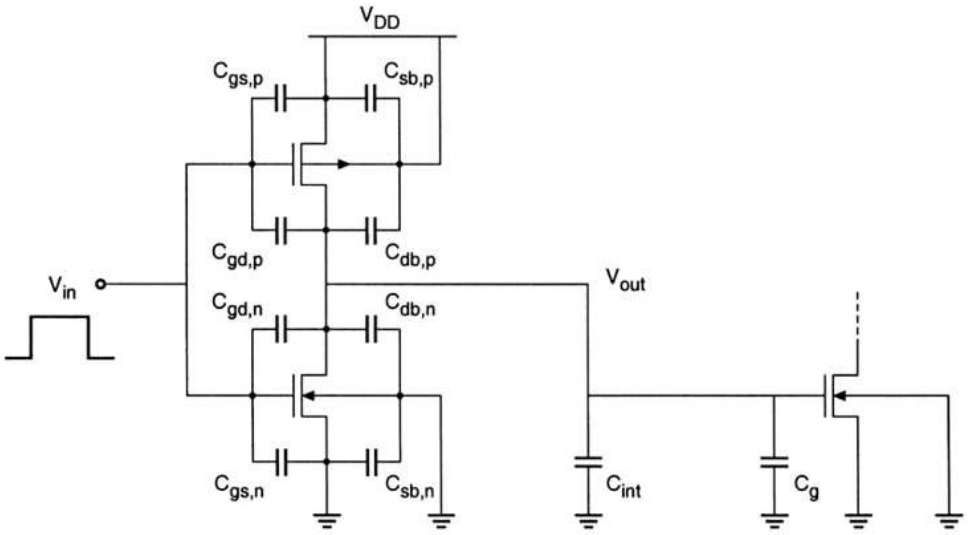
# ECE222 Midterm Examination on Oct. 24, 2019

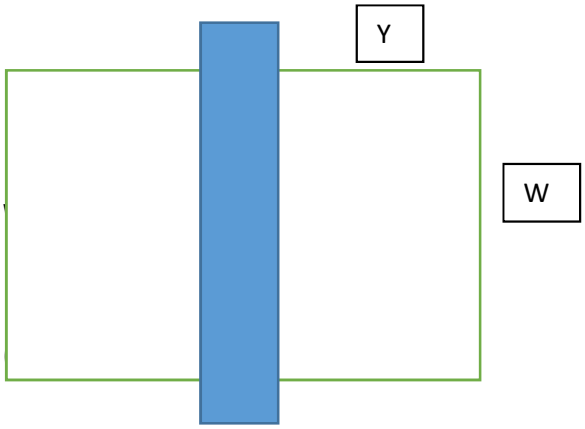
Name_____ Student ID_____

[1]. (30 points) A CMOS inverter diagram shows important parasitics in physical realization. The output node capacitance $C_{load}$ can be calculated as below.




$$C_{load} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_{int} + C_g$$

Let us assume that the vertical width (channel width) of NMOST is W = 6 μm, its horizontal dimension Y= 6 μm, the gate-to-drain overlap distance $L_D$= 10 nm, the gate oxide thickness $t_{ox}$= 1.6 nm, the doping of n-type diffusion $N_D$ = $2.10^{20}/cm^3$, the p-type substrate doping $N_A = 2.10^{20}$, the channel stop doping around n-type diffusion periphery = 16 X p-type doping ( $N_A = 2.10^{20}$), the junction depth (abrupt) $X_j$ = 32 nm.



$(a).\,(15\ \text{points})$ Assume zero interconnect capacitance, i.e., $C_{int}$=0, $C_{gd,p}$= $2C_{gd,n}$, $C_{gb,p}$= $2C_{gb,n}$, and $C_g$ for L= 2 μm. The drain node voltage changes from 1.2 V to 0 V for the gate input voltage of 1.2 V**. Find $\boldsymbol{C_{load}}$ for output voltage 1.2V and 0V.**

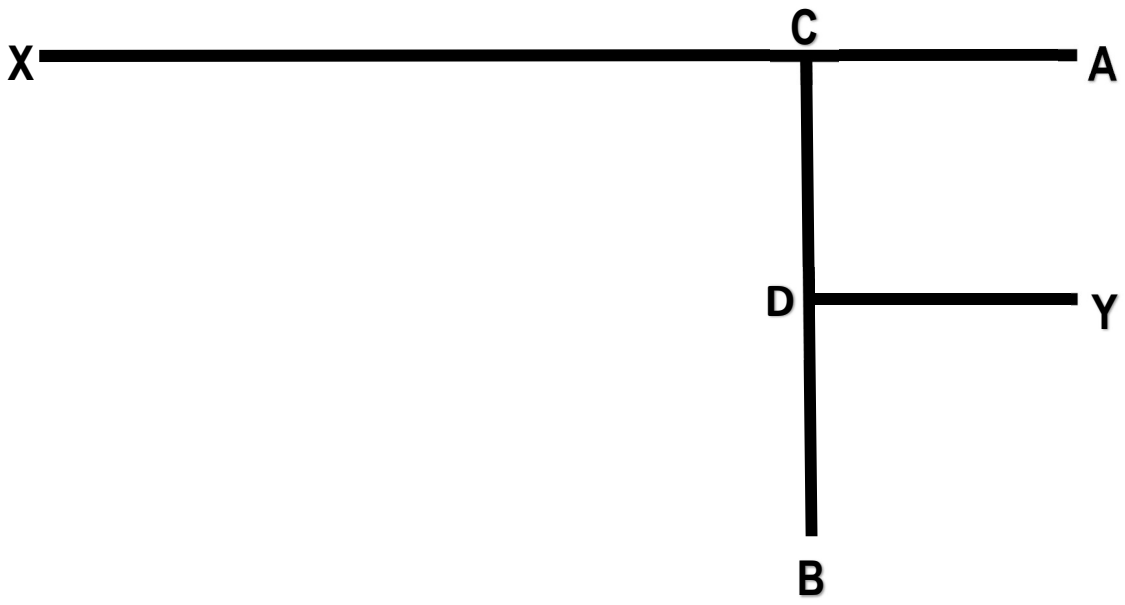
Hint: $C_{g,b}$= 0 for both linear and saturation, $C_{g,d}$= 0.5 X $C_{ox}$WL + $C_{ox}$W$L_D$ in linear mode and $C_{g,d}$= $C_{ox}$W$L_D$ in saturation mode, and $C_{gs\ (total)}$= 0.5 X $C_{ox}$WL + $C_{ox}$W$L_D$ in linear region and 2/3 $C_{ox}$WL + $C_{ox}$W$L_D$ in saturation region.

(b).(15 points) Let $V_{T0}$= 0.53 V. Also, measured I-V characteristics for NMOST with W= 6 μm, $E_C$L= 0.4V, λ= 0.05, 2$\Phi_F$= -1.1V are

| $V_{GS}$ | $V_{DS}$ | $V_{SB}$ | $I_{DS}$ (mA) |
|---|---|---|---|
| 0.6 | 0.6 | 0.0 | 0.06 |
| 0.65 | 0.6` | 0.0 | 0.12 |
| 0.9 | 1.2 | 0.3 | 0.44 |
| 1.2 | 1.2 | 0.3 | 1.56 |

**Calculate the fall time delay $t_f$ as time taken for the output node voltage changing from 1.2V to 0.6V for the gate input voltage of 1.2V using $C_{load}$ found in Part (a).**

[2]. (20 points) In VLSI circuits in nanoscale, interconnect delays have become speed bottlenecks. Let us consider a long interconnect wire tree shown below.




Information on interconnects:

Wire width (uniform) W = 1.0 μm, wire thickness (t) = 0.25 μm,

Length (L): X-C = 750 μm, C-A = 250 μm, C-D = 250 μm, D-Y = 250 μm, D-B = 250 μm.

The resistivity of the wire ρ = 0.01 [Ω. μm] and wire resistance for length L is

R= ρ . L / A, where A = the cross-sectional area ( t .W).

(a) (10 points) Draw a RC network for the interconnection tree above, Use a distributed model by representing lumped R, C parasitics for every 250 μm.
Use $C_{int}$= 0.1 fF/ μm.

(b). (10 points) **Find the X-Y delay by using the Elmore delay model.**

[3]. (20 points) In a 5nm technology node, a ring oscillator built with a chain 21 serially connected inverters of same size with an input gate capacitance of 50 fF generates a 100 GHz oscillation. In a critical path within a chip, the same size inverter as used in the ring oscillator is facing a 20pF capacitive load. **Design a supper buffer to minimize the delay and calculate the total delay.**

[4]. (10 points) Let us consider the principles of low power design, low energy-delay product while meeting delay specifications in VLSI design. For target speed as specified in terms of the clock frequency (e.g., 2.5 GHz), all timing critical paths need to meet the delay specifications, such as one or two clock period with some time margins.

(a). Describe your design method for reducing leakage currents with design variables $V_{DD}$, $V_{th}$, and transistor size W. For this problem, we assume that design problems can be solved without logic changes.

(a.1) (5 points) How would you meet the delay specifications in the critical paths?

(a.2) (5 points) Explain how you would you most effectively trade off energy vs. delay in general, for both critical and non-critical paths?

[5]. (20 points) In the Shannon's Limit Theorem, the minimum energy required for delivering binary information from one node to another node within a VLSI chip in terms of the channel capacity ( C ), the signal bandwidth (BW) of a signal path such as an interconnect line, the transmission rate ( R ), and the signal-to-noise ratio (SNR) is described as

$$C = BW\ log_2\ (1 + SNR).$$

Consider a logic gate driving a load capacitance $C_{load}$= 0.1 pF at a transmission rate (R) of 2.5 GHz. The signal path (line) is known to have a bandwidth (BW) of 25 GHz.

Energy required for delivering binary information to the load is

$$E_b = SNR.\ N_0.\ BW/R,$$

where $N_0$ = ½ $C_{load}$ . $v_n^2$ and $v_n$= average noise voltage

(a).(5 points) Calculate $E_b$ [J] for $v_n$= 500 μV and SNR=100.

(b).(15 points) Compare $E_b$ calculated in part (a) against the Shannon's Limit ½ kT ln 2, where k= 1.38 $10^{-2}$ [J/K] and T = 300K at room temperature. How much room is there in terms of performance improvement? Which one would you improve? If you increase the transmission rate R alone, how much more can you increase?