to 50%. A low-swing clock, double edge-triggered flip-flop has been developed by merging two power-saving techniques for the clock network.

Appendix

CMOS Schmitt Trigger DC analysis
vdd 1.2 0 dc 1.2V
vin 1 0 dc 1V
m5 2 1 0 0 mn l=60n w=1.8u
m4 3 1 2 0 mn l=60n w=1.2u
m6 5 3 2 0 mn l=60n w=180n
m1 4 1 5 5 mp l=60n w=1.8u
m2 3 1 4 5 mp l=60n w=720n
m3 0 3 4 5 mp l=60n w=180n
.model mn nmos vto=0.48 gamma=0.524 kp=1.05e-4 2phi_f=-1.011 Elump=0.4
.model mp pmos vto=-0.46 gamma=0.409 kp=5.1e-5 2phi_f=-0.972 Elump=1.8
.dc vin 0 1.2 0.01
.print dc v(0.8)
.end

We start our step-by-step analysis by considering a positive input sweep, i.e., assuming that the input voltage is increasing from 0 to \( V_{DD} \).

At \( V_i = 0 \) V: M1 and M2 are turned on, then

\[ V_x = V_y = V_{DD} = 1.2 \text{ V} \]

At the same time, M4 and M5 are turned off. M3 is off; M6 is on and operates in the saturation region. Assuming the threshold voltage of M6 with \( 2\phi_f = -1.011 \text{ V} \) is 0.62 V,

\[ V_z = V_{DD} - V_{th} = 0.58 \text{ V} \]
At $V_{in} = V_{T0,n} = 0.48$ V: M5 starts to turn on, M4 is still off.

$$V_z = 1.2 \text{ V}$$

At $V_{in} = 0.6$ V: Assume M4 is off, while both M5 and M6 operate in the saturation region. Also, let $E_{CL_n} = 0.4$ V.

$$\frac{k'_p}{2} \left( \frac{W}{L} \right)_5 \cdot \frac{E_{CL_n} \cdot (V_{in} - V_{T0,n})^2}{(V_{in} - V_{T0,n}) + E_{CL_n}} = \frac{k'_n}{2} \left( \frac{W}{L} \right)_6 \cdot \frac{E_{CL_n} \cdot (V_{DD} - V_z - V_{T0})^2}{(V_{DD} - V_z - V_{T0}) + E_{CL_n}}$$

$$0.4 \cdot (0.6 - 0.48)^2$$

$$0.6 - 0.48 + 0.4$$

$$= \left( \frac{1}{10} \right) \cdot 0.4 \cdot \left\{ 1.2 - V_z - \left[ 0.48 + 0.524 \left( \sqrt{1.011} + V_z - \sqrt{1.011} \right) \right] \right\}^2$$

$$= \left( \frac{1}{10} \right) \cdot 0.4 \cdot \left\{ 1.2 - V_z - \left[ 0.48 + 0.524 \left( \sqrt{1.011} + V_z - \sqrt{1.011} \right) \right] \right\} + 0.4$$

Solving this equation for $V_z$, we find that there is only one physically reasonable root.

$$V_z = 0.18 \text{ V}$$

Now, we check our assumption made above, i.e., M4 is indeed turned off.

$$V_{GS,4} = 0.6 - 0.18 = 0.42 < V_{T0,n} = 0.48$$

At $V_{in} = 0.62$ V: $V_z$ continues to decrease. Assuming M5 in linear region and M6 in saturation, we arrive at the following current equation:

$$\frac{k'_p}{2} \left( \frac{W}{L} \right)_5 \cdot \frac{1}{1 + \frac{V_z}{E_{CL_n}}} \cdot \left[ 2 \cdot (V_{in} - V_{T0,n}) \cdot V_z - V_z^2 \right]$$

$$= \frac{k'_n}{2} \left( \frac{W}{L} \right)_6 \cdot \frac{E_{CL_n} \cdot (V_{DD} - V_z - V_{T0})^2}{(V_{DD} - V_z - V_{T0}) + E_{CL_n}}$$

$$\frac{1}{1 + \frac{V_z}{0.4}} \cdot \left[ 2(0.62 - 0.48) \cdot V_z - V_z^2 \right]$$

$$= \left( \frac{1}{10} \right) \cdot 0.4 \cdot \left\{ 1.2 - V_z - \left[ 0.48 + 0.524 \left( \sqrt{1.011} + V_z - \sqrt{1.011} \right) \right] \right\}^2$$

$$= \left( \frac{1}{10} \right) \cdot 0.4 \cdot \left\{ 1.2 - V_z - \left[ 0.48 + 0.524 \left( \sqrt{1.011} + V_z - \sqrt{1.011} \right) \right] \right\} + 0.4$$

Solving this equation for $V_z$, we obtain, $V_z = 0.1$. Now determine the gate-to-source voltage of M4 as

$$V_{GS,4} = 0.62 - 0.1 = 0.52 \text{ V} > V_{T,n4} = 0.51$$

It is seen that at this point, M4 is already on. Thus, the previous analysis, which is based on the assumption that M4 is not conducting, can no longer be valid. At this input voltage, node x is being pulled down toward “0.” This can also be seen clearly from the simulation results. We conclude that the upper logic threshold voltage $V_{th+}$ is approximately equal to 0.62 V.
Next, we consider a negative input sweep, i.e., assume that the input voltage is decreasing from $V_{DD}$ to 0. At $V_{in} = 1.2$ V: M4 and M5 are on, so that the output voltage is $V_s = 0$ V. The pMOS transistors M1 and M2 are off, and M3 is in saturation, thus,

\[
\frac{k_p'}{2} \left( \frac{W}{L} \right) \frac{E_{CL_p} \cdot (0 - V_s - V_{T,3})^2}{(0 - V_s - V_{T,3}) + E_{CL_p}} = 0
\]

\[
V_y = -V_{T,3} = -\left[ V_{th,p} - 0.406 \left( \sqrt{0.972 + V_{DD} - V_y} - \sqrt{0.972} \right) \right]
\]

\[
V_y = 0.573 \text{ V}
\]

At $V_{in} = 0.74$ V: M1 is at the edge of turning on, M2 is off, and M3 is in saturation. The output voltage is still unchanged.

At $V_{in} = 0.6$ V: M1 is on and in saturation region. M3 is also in saturation, thus,

\[
\frac{k_p'}{2} \left( \frac{W}{L} \right) \frac{E_{CL_p} \cdot (V_{in} - V_{DD} - V_{th,p})^2}{(V_{in} - V_{DD} - V_{th,p}) + E_{CL_p}} = \frac{k_p'}{2} \left( \frac{W}{L} \right) \frac{E_{CL_p} \cdot (0 - V_s - V_{T,3})^2}{(0 - V_s - V_{T,3}) + E_{CL_p}}
\]

\[
1.8 \cdot \frac{0.6 - 1.2 - (-0.46))^2}{[0.6 - 1.2 - (-0.46)] + 1.8}
\]

\[
= \left( \frac{1}{10} \right) \cdot 1.8 \cdot \left[ \frac{0 - V_y - [-0.46 - 0.406 \left( \sqrt{0.972 + 1.2 - V_y} - \sqrt{0.972} \right)]}{0 - V_y - [-0.46 - 0.406 \left( \sqrt{0.972 + 1.2 - V_y} - \sqrt{0.972} \right)]} + 1.8
\]

The solution of this equation yields

\[
V_y = 0.92 \text{ V}
\]

Now we determine the gate-to-source voltage of M2 as

\[
V_{GS,2} = 0.6 - 0.92 = -0.32 > V_{th,p} = -0.46
\]

which indicates that M2 is still turned off at this point.

At 0.52 V: If M2 is still off, M1 is in the linear region, and M3 is in the saturation region:

\[
\frac{k_p'}{2} \left( \frac{W}{L} \right) \frac{1}{1 + \frac{V_y}{E_{CL_p}}} \cdot \left[ 2 \cdot (V_{in} - V_{DD} - V_{th,p}) - (V_s - V_{DD}) - (V_y - V_{DD})^2 \right]
\]

\[
= \frac{k_p'}{2} \left( \frac{W}{L} \right) \frac{E_{CL_p} \cdot (0 - V_s - V_{T,3})^2}{(0 - V_s - V_{T,3}) + E_{CL_p}}
\]

\[
= \left( \frac{1}{10} \right) \cdot 1.8 \cdot \left[ 0 - V_y - [-0.46 - 0.406 \left( \sqrt{0.972 + 1.2 - V_y} - \sqrt{0.972} \right)] \right]
\]

\[
= \left( \frac{1}{10} \right) \cdot 1.8 \cdot \left[ \frac{0 - V_y - [-0.46 - 0.406 \left( \sqrt{0.972 + 1.2 - V_y} - \sqrt{0.972} \right)]}{0 - V_y - [-0.46 - 0.406 \left( \sqrt{0.972 + 1.2 - V_y} - \sqrt{0.972} \right)]} + 1.8
\]
Figure A.1 Simulated output voltage waveforms of the CMOS Schmitt trigger circuit, for increasing and for decreasing input voltage.

Solving this quadratic equation yields

\[ V_f = 0.98 \, \text{V} \]

It can be shown that at this point, the pMOS transistor M2 is already turned on. Consequently, the output voltage is being pulled up to \( V_{DD} \). We conclude that the lower logic threshold voltage \( V_{th} \) is approximately equal to 0.52 V.

The SPICE simulation results are plotted in Fig. A.1 for both increasing and decreasing input voltages. The expected hysteresis behavior and the two switching thresholds are clearly seen in the simulation results.

Exercise Problems

8.1 Figure P8.1 shows a schematic for a positive edge-triggered D flip-flop. Use a layout editor (e.g., Magic) to design a layout of the circuit. Use CMOS technology, and assume that you have n-type substrate. On the printout of your layout, clearly indicate the location of each logic gate in the figure. Also, calculate the parasitic capacitances of your layout.

- \( W_n = 4 \, \mu\text{m} \) and \( W_p = 8 \, \mu\text{m} \) for all gates
- \( L_M = 2 \, \mu\text{m} \)
- \( L_D = 0.25 \, \mu\text{m} \)
- \( V_{T0,n} = 1 \, \text{V} \)
- \( V_{T0,p} = -1 \, \text{V} \)
- \( k_n = 40 \, \mu\text{A/V}^2 \)
- \( k_p = 25 \, \mu\text{A/V}^2 \)
- \( t_{ox} = 20 \, \text{nm} \)

8.2 For the rise time \( t_{r} \) and fall time \( t_{f} \) of the D flip-flop, obtain (a) a plot of the signal waveforms.

a. A plot for a small input transition
b. A plot for a large input transition
c. A plot for a reverse-gating transition
d. A plot for a reverse-Going transition

8.3 We have an appendix circuit diagram with rise and fall delays that we wish to reverse with SPICE. We wish to simulate this using SPICE. We wish to simulate an inverter using inverters with a transition voltage of 0.5 V. The simulation results are plotted in Fig. A.1 for both increasing and decreasing input voltages. The expected hysteresis behavior and the two switching thresholds are clearly seen in the simulation results.

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