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A Design of CMOS Polycells for LSI Circuits

SUNG MO KANG

Abstract— **We have designed CMOS polycells with a uniform height for LSI random logic circuits. The design objective was to minimize the product of propagation delay and chip area while allowing noise margins to be at least 25 percent of V_{dd}. Designable parameters were identified to be channel widths in p-type and n-type transistors. Analytical models were derived to show the existence of an optimal solution point. Physical interpretations of models were also given. SPICE was used to simulate propagation delays and noise margins in inverter (INR), 2- and 3-input NAND and NOR gates under worst-case conditions. The chip performance of polycell-based CMOS circuits was then estimated by averaging performances of these five logic gates. With 3.5-μm design rules, the channel widths in p-channel and n-channel transistors were designed to be 35 μm and 17 μm, respectively.**

NOMENCLATURE

$C_{A(p)}, C_{A(n)}$	Capacitance per unit area in p- and n-diffusion ($pF/\mu m^2$).
C_L	Load capacitance (pF).
C_{ox}	Gate capacitance per unit area ($pF/\mu m^2$).
$C_{p(p)}, C_{p(n)}$	Capacitance per unit perimeter in p- and n-diffusion are ($pF/\mu m$).
D_d	Diffusion width in the drain area (μm).
fo	Number of fanouts.
K_{ox}	Relative permittivity of the silicon dioxide (3.9).
L_p, L_n	Gate channel length in p- and n-channel transistors (μm).
t_{ox}	Gate oxide thickness (Å).
$V_{th(p)}, V_{th(n)}$	Threshold voltage in p- and n-channel transistors (V).
W_p, W_n	Gate channel width in p- and n-channel transistors (μm).
ϵ_0	Permittivity of free space (8.854×10^{-14} F/cm).
μ_p, μ_n	Mobility of minority carriers in p- and n-channel transistors ($cm^2/V\cdot s$).

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The author is with Bell Laboratories, Murray Hill, NJ 07974.

I. INTRODUCTION

MOS (Metal–Oxide–Silicon) polycells are often used as building blocks of large-scale random logic integrated circuits to achieve a fast turnaround time. Although known to have some chip area penalty, the polycell-based design approach allows significant savings in design efforts and time. With availability of a polycell library that provides information on propagation delay time and layout of each polycell, logic designers can come up with "reasonably wishful" timing specifications by estimating delay times in critical paths. The circuit designer's task then involves optimally placing and interconnecting from several hundred to a few thousand polycells subject to various timing specifications.

This paper is addressed to LSI Complementary MOS (CMOS) polycell design problems. As is well known, any rigorous electronic circuit design requires optimization of multiple criteria. Recently Fraser, Director, and Lightner [1]–[4] have formulated general circuit design problems and applied multiple criterion optimization techniques to design some logic gates. Usually design objectives specified in terms of power dissipation, chip area, propagation delay and noise margins are conflicting and some trade-offs need to be made among them. In [1]–[4] a weighted p-norm of design objectives was used as a cost function and optimization procedures were developed to determine proper weights as well as design parameters.

The problem of designing LSI polycells is quite different from those in customized special gate designs. Although each polycell can be designed independently based on its design objectives, such a set of polycells is not always optimal for LSI circuits, especially when the efficiency or routing measured in terms of chip area is an important issue. Also in the polycell design, some regularity in layout style needs to be maintained. Without some regularity in layout style, a significant amount of chip area is often sacrificed not to violate design rules such as the minimum separations between thinox regions corresponding to sources and drains of p- or n-type transistors. Usually a uniform height is used for all polycells. This uniform height allows easy routing of power bus lines internal to polycells and helps to fully utilize the routing domain [5]. Fig. 1 shows a typical polycell layout of 2-input NAND gate for illustration. To minimize parasitic capacitances, the horizontal pitch between polysilicon gates is kept at minimum as determined by design rules on the minimum window size and the spacing between the window and polysilicon gate edge. Therefore, it is clear that major design parameters in CMOS polycells with a uniform height are channel widths in p- and n-type transistors denoted by W_p and W_n. In Fig. 1 the separation between p-channel and n-channel transistors is denoted by S.

II. DESIGN OBJECTIVE

An often-discussed performance measure of integrated circuits is the product of power dissipation and propagation delay. This product is regarded important since it represents the dissipated energy per switching operation [6]. An equally important measure

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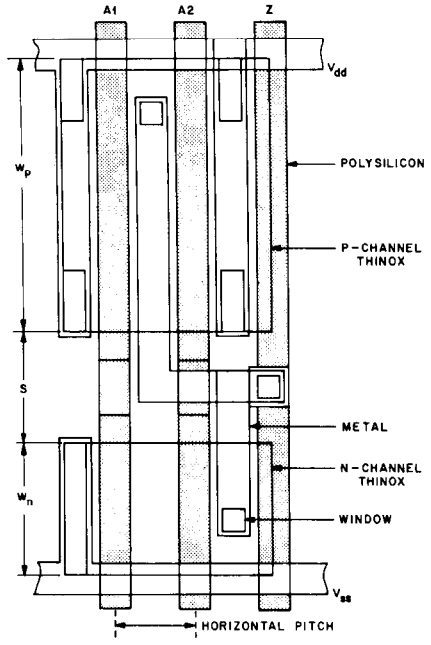

Fig. 1. A typical layout of a CMOS polycell NAND2 with output $Z=\overline{A1\cdot A2}$.

is the chip area since the production yield of LSI chips decreases rapidly as chip area increases [7]. Besides, the chip area is closely related to speed since, for a given technology, larger chips usually contain longer signal paths.

In CMOS circuits, power dissipation is small and so far has not been a limiting factor. Therefore, for CMOS polycell design, we will concentrate on propagation delay and chip area.

For a given technology, our design goal is to maximize the technology power by increasing on-chip functional events per unit time. Recently, Murphy [8] introduced a measure technology power (TP) of the form

$$\text{TP} \triangleq \frac{\text{number of logical nodes per chip}}{\text{loaded gate delay}}.$$

This measure can be conveniently used to evaluate performance advantages of bipolar, NMOS, CMOS or other technology. For instance, even though bipolar technology may yield the minimum gate delay, the number of logical nodes that can be put onto a single chip is severely limited by power dissipation. Therefore, this technology does not always give the best TP. In polycell-based CMOS circuits, we can maximize TP by minimizing the product of active chip area and propagation delay since the number of logical nodes on a chip is inversely proportional to the active chip area occupied by polycells. To ensure noise immunity of LSI circuits at 5 V and below, we have required noise margins to be at least 25 percent of V_{dd}.

III. Basic Assumptions

For polycell design, we make the following basic assumptions:

1) Circuit performance of a polycell-based CMOS LSI chip may be represented by a set of inverter (INR), 2- and 3-input NAND and NOR gates (henceforth, denoted by NAND2, NOR2, NAND3 and NOR3).

2) On the average, the fanout of each gate is three and the routing distance for each fanout is approximately 70 horizontal pitches.

3) The worst-case ambient temperature is 85°C and power supply voltage V_{dd} is 5 V $\pm$ 5 percent.

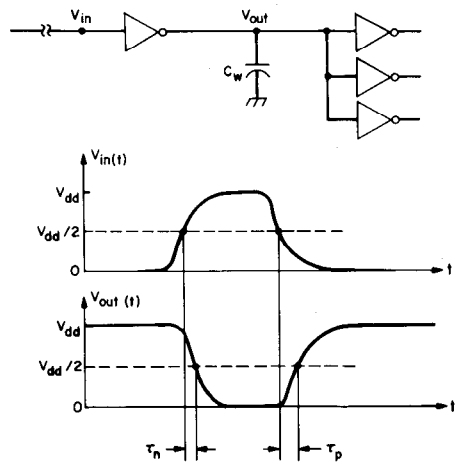

Fig. 2. Fifty-percent point propagation delays in n-channel (τ_n) and p-channel (τ_p) in CMOS inverter (INR) with fanout = 3.

4) For CMOS LSI chips, power dissipation is not a limiting factor.

In the following sections, we will derive analytical expressions for propagation delay times and effective chip area of an "average" polycell in terms of design parameters W_p and W_n. Then we will show that our objective function, i.e., the delay-area product, is concave and, therefore, has a solution point. To determine optimal values for W_p and W_n, SPICE [9] will be used to simulate propagation delays and noise margins in aforementioned five logic gates under worst-case conditions.

IV. Propagation Delays in CMOS Gates

In this paper, the propagation delay of an individual gate is determined by averaging 50-percent point delay times in n-channel (τ_n) and p-channel (τ_p), as shown in Fig. 2. For gates with more than one input, we will assume that only one input changes its state at any given time and all other inputs will be set at V_{dd} for NAND gates or $V_{ss}=0$ for NOR gates.

Propagation delay times τ_n and τ_p decrease as current-driving capability of the driver (proportional to gate channel widths W_n and W_p) increases, whereas they increase with capacitive loading which consists of the drain capacitance in the driver (C_0), the interconnection-wire capacitance (C_w) and the total input capacitance of fanout gates (C_i). Propagation delay times also depend on input waveforms. Usually input waveforms with shorter rise and fall times yield less propagation delay. Therefore, the functional relationships between propagation delays and important circuit parameters can be described by

$$\begin{aligned}\tau_n &= f(W_n, C_0 + C_w + C_i; V_{\text{in}}(\cdot)) \\ \tau_p &= g(W_p, C_0 + C_w + C_i; V_{\text{in}}(\cdot)) \end{aligned} \quad (1)$$

where $V_{\text{in}}(\cdot)$ denotes the input waveform and C_0, C_w, and C_i are implicit functions of W_n and W_p.

Since we measure propagation delays in multiinput gates with all inputs except one set as either V_{dd} or zero, multiinput gates can be considered as "modified" inverters. Fig. 3 shows equivalent circuit representations of NAND3 and NOR3 with their two inputs set at V_{dd} and zero, respectively. Basically nonlinear RC circuits in n-channel of NAND3 and p-channel of NOR3 act as delay elements and increase both τ_n and τ_p.

The effect of W_n and W_p on τ_n and τ_p can be best illustrated through the INR circuit shown in Fig. 4. Assuming that the input

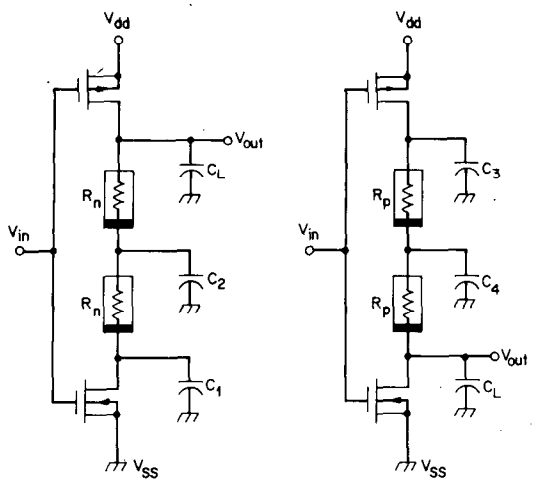

Fig. 3. Equivalent circuits for (a) NAND3, and (b) NOR3 with their two inputs set at V_{dd} and $V_{ss}=0$, respectively.

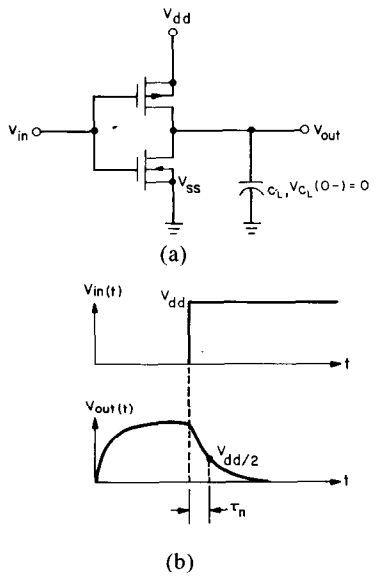

Fig. 4. (a) A CMOS inverter circuit. (b) Its input–output signal pair.

voltage $V_{in}(t)$ has an "ideal" pulse waveform for simplicity, we can derive an analytical expression for τ_n from the following state equations:

NFET in saturation ($V_G - v_{out} \leq V_{th(n)}$):

$$C_L \frac{dv_{out}}{dt} = -\beta_n (V_G - V_{th(n)})^2. \tag{2.a}$$

NFET in linear region ($V_G - v_{out} > V_{th(n)}$):

$$C_L \frac{dv_{out}}{dt} = -\beta_n \left(2(V_G - V_{th(n)})v_{out} - v_{out}^2\right) \tag{2.b}$$

where

$$\beta_n = \frac{\mu_n W_n C_{ox}}{2L_n}$$

$$C_{ox} = \frac{K_{ox}\epsilon_0}{t_{ox}}.$$

The time interval for the NFET to remain in saturation denoted by t_s can be obtained from (2.a):

$$C_L \int_{V_{dd}}^{V_{dd}-V_{th(n)}} dv_{out} = -\beta_n (V_{dd} - V_{th(n)})^2 \int_0^{t_s} dt. \tag{3}$$

Solving (3) for t_s yields

$$t_s = \frac{V_{th(n)}}{\beta_n (V_{dd} - V_{th(n)})^2} C_L. \tag{4}$$

The time interval for the NFET to stay in the linear region until it reaches one half of V_{dd} is obtained from (2.b):

$$C_L \int_{V_{dd}-V_{th(n)}}^{\frac{1}{2}V_{dd}} \frac{dv_{out}}{2(V_{dd} - V_{th}(n))v_{out} - v_{out}^2} = -\beta_n \int_{t_s}^{\tau_n} dt \tag{5}$$

and, therefore, the propagation delay in the n-channel transistor τ_n has the form

$$\tau_n = \frac{C_L}{\frac{\mu_n}{2}\frac{W_n}{L_n}\frac{K_{ox}\epsilon_0}{t_{ox}}} \left[\frac{V_{th(n)}}{(V_{dd} - V_{th(n)})^2} + \frac{1}{2(V_{dd} - V_{th(n)})} \cdot \ln\left(\frac{1.5V_{dd} - 2V_{th(n)}}{0.5V_{dd}} \right) \right]. \tag{6}$$

Similarly, τ_p can be expressed by (6) with subscript n replaced by p.

For m-input NAND and NOR gates, propagation delays in p-channel and n-channel can be approximated by [10]

$$\begin{aligned} \tau_p(\text{NAND}m) &= \tau_p \\ \tau_p(\text{NOR}m) &= m\tau_p \\ \tau_n(\text{NAND}m) &= m\tau_n \\ \tau_n(\text{NOR}m) &= \tau_n. \end{aligned} \tag{7}$$

Therefore, if we let $\tau_n^{(j)}$ and $\tau_p^{(j)}$ denote the propagation delays in the jth polycell among the five as ordered in assumption 1, then the mean delay time in an "average" polycell can be expressed by

$$\begin{aligned} \bar{\tau} &= \frac{1}{N} \sum_{j=1}^{N=5} \frac{1}{2}\left(\tau_p^{(j)} + \tau_n^{(j)}\right) \\ &= \frac{1}{5} \cdot \frac{1}{2}\left(\tau_p + \tau_p + 2\tau_p + \tau_p + 3\tau_p + \tau_n + 2\tau_n + \tau_n + 3\tau_n + \tau_n\right) \\ &= \left(K_n \frac{1}{\mu_n W_n} + K_p \frac{1}{\mu_p W_p} \right) C_L \end{aligned} \tag{8}$$

where

$$K_z = \frac{1.6 L_z t_{ox}}{K_{ox}\epsilon_0} \left[\frac{V_{th(z)}}{(V_{dd} - V_{th(z)})^2} + \frac{1}{2(V_{dd} - V_{th(z)})} \cdot \ln\left(\frac{1.5V_{dd} - 2V_{th(z)}}{0.5V_{dd}} \right) \right]$$

for $z=n$ or p. The load capacitance C_L can be expressed by

$$\begin{aligned} C_L &= C_0 + C_w + C_i \\ &= (C_{A(p)}W_p + C_{A(n)}W_n)D_d + 2(W_p + D_d)C_{p(p)} \\ &\quad + 2(W_n + D_d)C_{p(n)} + C_w(W_p, W_n) + \text{fo}(W_p L_p + W_n L_n)C_{ox}. \end{aligned} \tag{9}$$

For simplicity, we assume that the interconnection-wire capaci-

tance (C_w), remains constant as we vary W_p and W_n. In reality, any change in C_w due to changes in W_p or W_n is small and, hence, this assumption is reasonable.

As mentioned earlier, the horizontal pitch between polysilicon gates is always kept at minimum to reduce parasitic capacitances. Therefore, the number of horizontal pitches that each logic gate takes is well fixed. For instance, INR takes only 2 pitches while NAND2 and NOR2 take 3 pitches, and NAND3 and NOR3 take 4 pitches. For this reason, the effective chip area for an "average" polycell can be represented by

$$A = W_p + W_n + S \tag{10}$$

where S denotes the spacing between p-channel and n-channel thinox regions specified by design rules. From (8) to (10), the product of propagation delay and chip area, henceforth called the objective function, can be written as

$$H(W_p, W_n) \triangleq A \cdot \bar{\tau} = (W_p + W_n + S)\left(K_n \frac{1}{\mu_n W_n} + K_p \frac{1}{\mu_p W_p}\right) \cdot (\alpha_p W_p + \alpha_n W_n + \alpha_0) \tag{11}$$

where

$$\alpha_z = C_{A(z)} D_d + 2C_{p(z)} + \text{fo} \cdot C_{ox} \cdot L_z, \qquad \text{for } z = p \text{ or } n$$
$$\alpha_0 = 2D_d\left(C_{p(p)} + C_{p(n)}\right) + C_w.$$

It can be shown from (11) that the objective function $H(W_p, W_n)$ is concave in W_p and W_n. For a given W_p, the product term can be rewritten as

$$H(W_n; W_p) = a_2 W_n^2 + a_1 W_n + a_0 + a_{-1} \frac{1}{W_n} \tag{12}$$

which is concave in W_n. Similarly, it can be shown that $H(W_p; W_n)$ is concave in W_p.

V. Consideration of Noise Margins

The noise margins of a logic gate is defined as the input voltage differences between the dc operating points and their nearest unity gain points [11]. Without sufficient noise margins, cross couplings between adjacent metal or polysilicon lines on the chip or from external environment may cause erroneous outputs. As design rules shrink, such cross couplings tend to increase and the consideration of noise margins becomes an important factor [8].

For a typical INR gate, its dc transfer characteristics can be calculated by using V–I characteristic equations of p-channel and n-channel transistors. In particular, the input gate voltage at which both p-channel and n-channel transistors operate in saturation can be expressed by [12]

$$V_{i(\text{sat})} = \frac{\sqrt{\beta_R}\left[V_{dd} - V_{th(p)}\right] + V_{th(n)}}{1 + \sqrt{\beta_R}} \tag{13}$$

where

$$\beta_R = \frac{\mu_p W_p}{\mu_n W_n}.$$

Equation (13) suggests that when $V_{th(n)} = V_{th(p)}$, the midtransition point can be centered at $V_{dd}/2$ to allow larger noise margins by setting

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}. \tag{14}$$

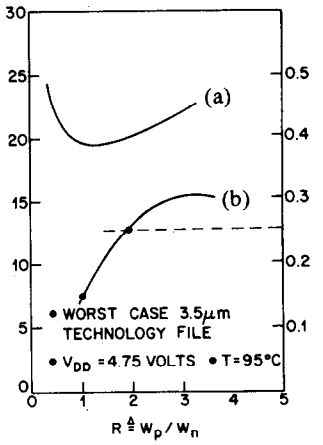

Fig. 5. (a) The propagation delay (ns) of an average logic gate. (b) The worst-case noise margin/V_{dd} versus the aspect ratio $R \triangleq W_p/W_n$.

In other words, for maximum noise margins, W_p should be about three times of W_n for the effective channel mobility carriers in n-channel is about three times that in p-channel.

VI. Worst-Case Simulations and Polycell Design

It is well known that transistor characteristics often depart from their nominal values due to processing variations. To check whether the design would meet the performance specifications, SPICE simulations were done under worst-case conditions to calculate propagation delays and dc transfer characteristics.

Worst-case device parameters that yield a low-current driving capability and, therefore, longer propagation delays were fed into SPICE through a so-called "worst-case technology file." Also the power supply voltage V_{dd} was set at 4.75 V, 5 percent below its nominal value and the device junction temperature was set at 95°C to account for on-chip power dissipation although the ambient temperature was assumed to be 85°C. Two extreme cases were considered to ensure sufficient noise margins, especially in low voltage operations with $V_{dd} = 2$ V. One extreme case was simulated with high-current p-channel and low-current n-channel device parameters and the other extreme case with low-current p-channel and high-current n-channel device parameters.

Fig. 5 illustrates the simulation approach that we used to achieve our design goal using 3.5-μm design rules and worst-case device parameters.

Simulation results shown in Fig. 5 were obtained with $W \triangleq W_p + W_n = 52$ μm. Curve (a) represents the average of worst-case propagation delays in INR, NAND2, NOR2, NAND3, and NOR3 for different aspect ratios between W_p and W_n while curve (b) shows worst-case noise margins. Curve (b) suggests that the aspect ratio $R \triangleq W_p/W_n$ should not be less than 2 in order to ensure the worst-case noise margin to be 25 percent of V_{dd}. Although the maximum noise margin can be achieved by setting $R = 3$, such a choice is not desirable for the minimum propagation delay occurs for R between 1 and 2. Since our design goal is to minimize the delay-area product and thereby to maximize the technology power, we chose $R = 2$ to avoid degrading the switching speeds of CMOS polycells. Figs. 6 and 7 show dc transfer characteristic curves with $W_p/W_n = 1$ and $W_p/W_n = 2$, respectively. At $V_{dd} = 2$ V, the noise margin can be as low as 0.3 V with $W_p/W_n = 1$, whereas the worst-case noise margin is about 0.5 V with $W_p/W_n = 2$. It can be observed that dc characteristic curves shift to the right as the aspect ratio R increases and achieves the maximum noise margin at $R = 3$.

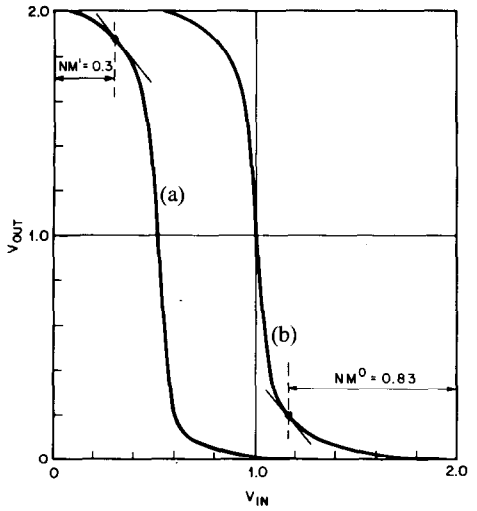

Fig. 6. DC transfer characteristics of INR with $W_p/W_n=26/26$. (a) High-current n-channel and low-current p-channel parameters. (b) Low-current n-channel and high-current p-channel parameters.

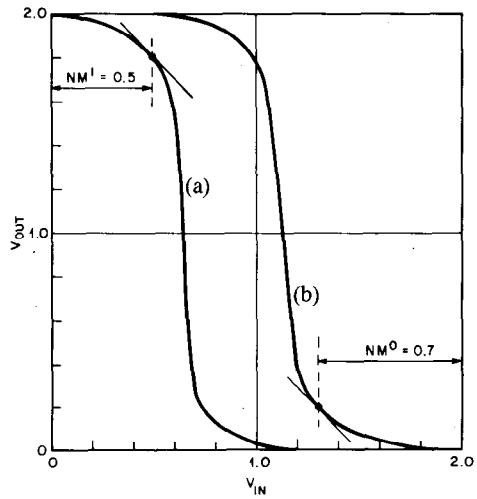

Fig. 7. DC transfer characteristics of INR with $W_p/W_n=35/17$. (a) High-current n-channel and low-current p-channel parameters. (b) Low-current n-channel and high-current p-channel parameters.

Having determined that the aspect ratio R should be 2, we next determine channel widths W_p and W_n that minimize the delay-area product. As shown in Fig. 8, the propagation delay decreases with increasing channel widths at the cost of chip area. Note that with a chosen aspect ratio $R=2$, our problem now becomes a one-dimensional search. In fact, (11) can be rewritten in terms of the total channel width W as

$$H(W)\triangleq A\cdot\bar{\tau}=(W+S)\cdot\frac{\alpha_{-1}}{W}(\alpha_1 W+\alpha_0) \qquad (15)$$

where

$$\alpha_{-1}=\frac{K_n}{\mu_n}(R+1)+\frac{K_p}{\mu_p}\frac{R+1}{R}$$

$$\alpha_1=\alpha_p\frac{R}{R+1}+\frac{\alpha_n}{R+1}.$$

In (15), the chip area A is an affine function of W and the mean propagation delay is composed of a fixed term and a term that is inversely proportional to W. Therefore, for small values of W, the speed improvement is quite noticeable as W increases

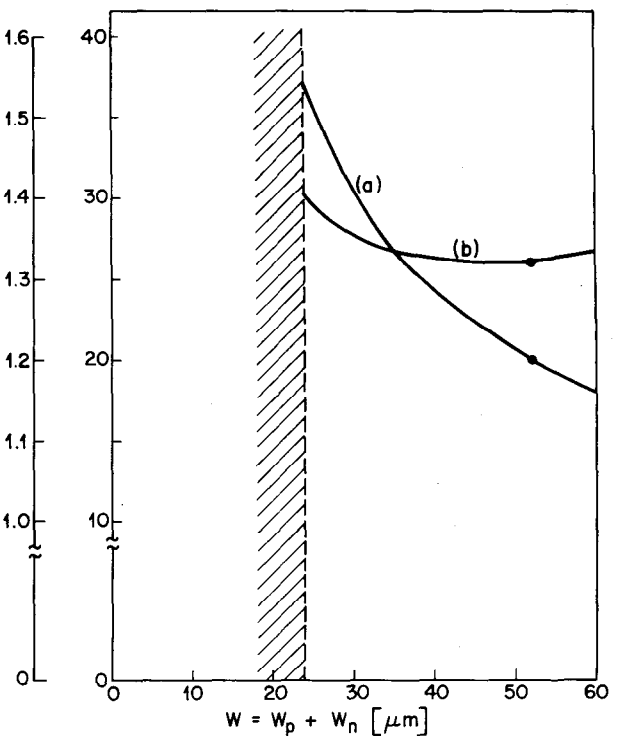

Fig. 8. (a) The average-gate propagation delay (ns). (b) The delay time-chip area product (10^{-12}s·m^2) versus the total channel width $W=W_p+W_n$.

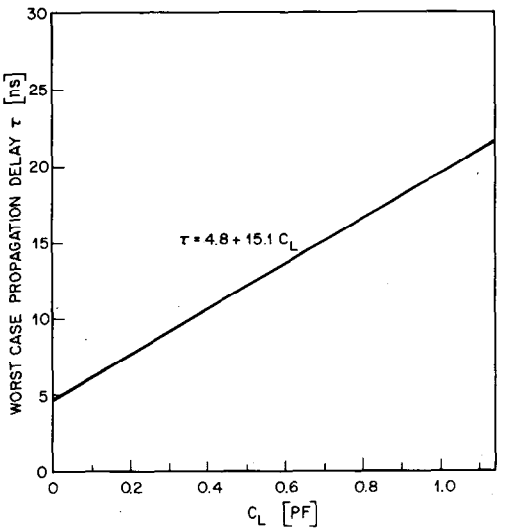

Fig. 9. The worst-case propagation delay of an "average" polycell gate versus capacitive loading C_L.

while the increase in chip area is small. Physically, it is indeed necessary to increase transistor sizes beyond the minimum size to overcome capacitive loadings from interconnection wires. Without routing capacitances, the best design would be to use minimum size transistors. On the other extreme, if the transistor sizes became excessively large, the gate loading from fanout gates would be dominant over routing capacitances and the propagation delay would remain almost constant leaving the increase in chip area unjustified. Indeed SPICE simulation well supports our model in (15) and finds the minimum point on curve (b) at $W=52$ μm. The shaded region in Fig. 8 is not accessible due to

design rules. This design yields the sizes of p-channel and n-channel transistors to be $W_p = 35$ μm and $W_n = 17$ μm. It also allows up to six metal wiring tracks internal to polycells. Fig. 9 shows the worst-case propagation delays in polycell circuits for different values of capacitive load C_L.

VII. Summary and Concluding Remarks

In this paper, we have considered a design of CMOS polycells for LSI random logic circuits. Our design objective was to minimize the delay-area product allowing sufficient noise margins under worst-case conditions. This design objective is in line with the goal of maximizing technology power and, thereby, fully increasing on-chip functional events per unit time. We have identified that designable parameters in CMOS polycells with a uniform height are channel widths in p- and n-type transistors denoted by W_p and W_n. Also, we derived an analytical expression for the design objective function in terms of designable parameters W_p and W_n. We then showed the concavity of the objective function to prove the existence of a solution point. Also a clear physical interpretation of our model was given in detail.

SPICE was used to calculate worst-case propagation delays and noise margins in inverter (INR), 2- and 3-input NAND and NOR gates with an average fanout of three. We assumed that the routing distance of each fanout was about 70 horizontal pitches. The power supply voltage V_{dd} was 5 V$\pm$5 percent and the ambient temperature was assumed to be 85°C. With 3.5 μm design rules, polycells were designed to have 35 μm of p-channel transistor width and 17 μm of n-channel transistor width. This choice allows the worst-case noise margin to be at least 25 percent of V_{dd}. Although the material we presented in this paper deals with typical logic gates, other polycells can be conveniently designed with same design parameters except special polycells used for input–output (I/O) pads. Usually such I/O polycells need to be very big to provide sufficient current-driving capability. We can design buffers of different sizes by properly connecting transistors in parallel with a uniform height. If there were any logical node requiring more than average fanouts, such a node could be handled by using a high-power version of the driving polycell, which can also be implemented with a uniform height.

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Cascade Synthesis of Linear Phase Selective Filters

ISAM H. ZABALAWI

***Abstract*—A new procedure has been developed for the synthesis of a class of nonminimum phase functions. This class is widely encountered in the design of linear phase selective filters. The procedure is based upon the extraction of the pair of transmission zeros $\mp\sigma_0 + jw_0$ by a two-port network. The network consists of shunt capacitors, invariant frequency elements (imaginary resistors) and ideal immittance inverters. The resulting networks are of a conjugate symmetry.**

The synthesized prototype networks can be transformed easily for microwave applications.

I. Introduction

The conventional and the ordinary linear phase filters are characterized by minimum phase transfer functions [1]. That is neither the poles nor the zeros of these functions are permitted in the RHP plane. It has been discussed in [2] that the amplitude and the phase characteristics of a minimum phase function are related through the Hilbert's Transform and this explains the incompatibleness of the amplitude and the phase of these functions.

In FDM/FM communication systems, data transmission and systems utilizing pulses, the amplitude and the phase responses of the filtering devices are of similar importance. Minimum phase functions cannot provide selective amplitude and linear phase over most of the entire passband. Filters exhibiting selective amplitude response with small inband variation and very flat passband group delay were originally designed in equalization basis (external equalization) [3]. However, the modern technique for designing filters with combined amplitude and phase requirements is to use a general nonminimum phase transfer function. The approximation problem of constructing this class of transfer functions has been treated in [4] and is not going to be discussed here.

Several procedures are available in the technical literature for the synthesis of the aforementioned class of nonminimum phase transfer functions, e.g., [5]–[7] in a cascade form.

Some of the resulting networks are physically unrealizable where frequency dependent resistors and imaginary resistors [8] had been used. Furthermore some others are nonreciprocal and this limits the realization. More recently an attempt has been made in [9] to synthesize a general second-order zero producing

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The author is with the Electrical Engineering Department, Faculty of Engineering and Technology, The University of Jordan, Anman, Jordan.

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